STD 7000

7601A
7602A
7603A
7604A

TTL PORT CARDS

USER'S MANUAL

INTRODUCTION

This TTL Port Cards User's Manual consists of the following user's manuals:

- The 7601A, a TTL Input/Output Card
- The 7602A, a TTL Output Card
- The 7603A, a TTL Input Card
- The 7604A, a TTL Input/Output Card

Each individual manual is complete unto itself including tables of contents and figures. However, the cards are compatible within a system, so this manual provides an easy reference source for expanding the port capabilities of your system.

CONTENTS

Introduction

Foreword

7601A User's Manual

7602A User's Manual

7603A User's Manual

7604A User's Manual

Return for Repair/Warranty

ASCII Code Assignments

FOREWORD

This manual explains how to use four Pro-Log TTL cards: the 7601A, 7602A, 7603A, and 7604A. It is structured to reflect the answers to basic questions that you might ask about these cards. We welcome your suggestions on how we can improve our instructions.

These cards are part of the Pro-Log Series 7000 STD BUS hardware. Our products are modular, and they are designed and built with second-sourced parts that are industry standards. They provide industrial managers with the means of using their own people to control the design, production, and maintenance of products that use STD BUS hardware.

Pro-Log supports its products with thorough and complete documentation. Also, to provide maximum assistance to the user, we teach courses on how to design with and use microprocessors and the STD BUS products.

You may find the following Pro-Log documents useful in your work: the Microprocessor User's Guide and the Series 7000 STD BUS Technical Manual. If you would like to receive a free copy of each publication, please submit a request on your company letterhead.

STD 7000

7601A

TTL INPUT/OUTPUT CARD

USER'S MANUAL

CONTENTS

	Page
Figures	iv
Section 1 - Purpose and Main Features	1-1
Purpose	1-1
Features	1-1
Section 2 - Installation and Specifications	2-1
Installation	2-1
I/O Mapped Card Addressing	2-2
Changing the Port Address	2-2
IOEXP	2-3
Cabling	2-4
Specifications	2-5
STD BUS Interface	2-5
Port Interface	2-5
Timing	2-7
Section 3 - Operation and Programming	3-1
Operation	3-1
Section 4 - Operating Software	4-1
Section 5 - Maintenance	5-1
Reference Drawings	5-1

FIGURES

Figure		Page
1-1	7601A	1-1
1-2	Block Diagram	1-2
2-1	Installation	2-1
2-2	Location of Features	2-2
2-3	Address Selection Jumpers	2-3
2-4	Low-Profile Connector	2-4
2-5	Electrical and Environmental Specifications	2-5
2-6	7601A/STD BUS Interface Specifications	2-6
2-7	Read Timing	2-7
2-8	Write Timing	2-8
5-1	Schematic	5-2
5-2	Assembly	5-4

PURPOSE

The 7601A provides four 8-bit TTL buffered input ports and four 8-bit TTL latched output ports, 32 lines total of each. The I/O lines are noninverting and the outputs can drive 16 LSTTL loads (4 TTL loads). The card decodes eight address lines and the STD BUS IOEXP signal. Slip-on connectors allow mapping to any consecutive group of I/O addresses. The STD BUS SYSRESET* signal clears all output ports simultaneously.

FEATURES

- Four 8-bit input ports, 32 lines
- Four 8-bit output ports, 32 lines
- Outputs drive 16 LSTTL loads (4 TTL loads)
- Inputs present 4 LSTTL loads (1 TTL load)
- Occupies four consecutive I/O addresses
- Flexible I/O mapping
- +5V operation
- Universal processor compatibility

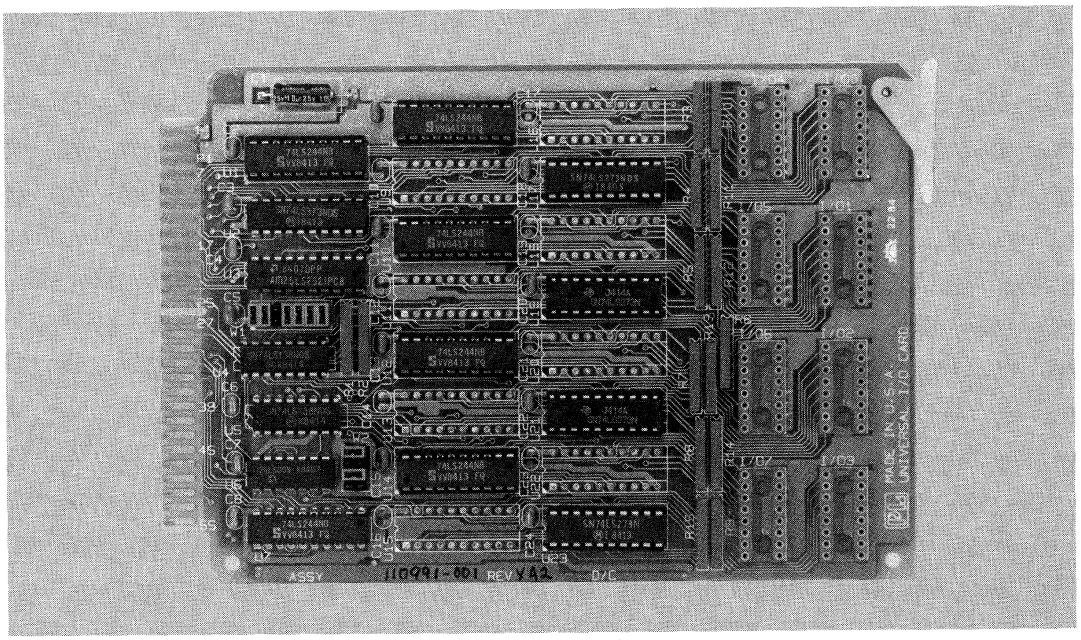


Figure 1-1. 7601A

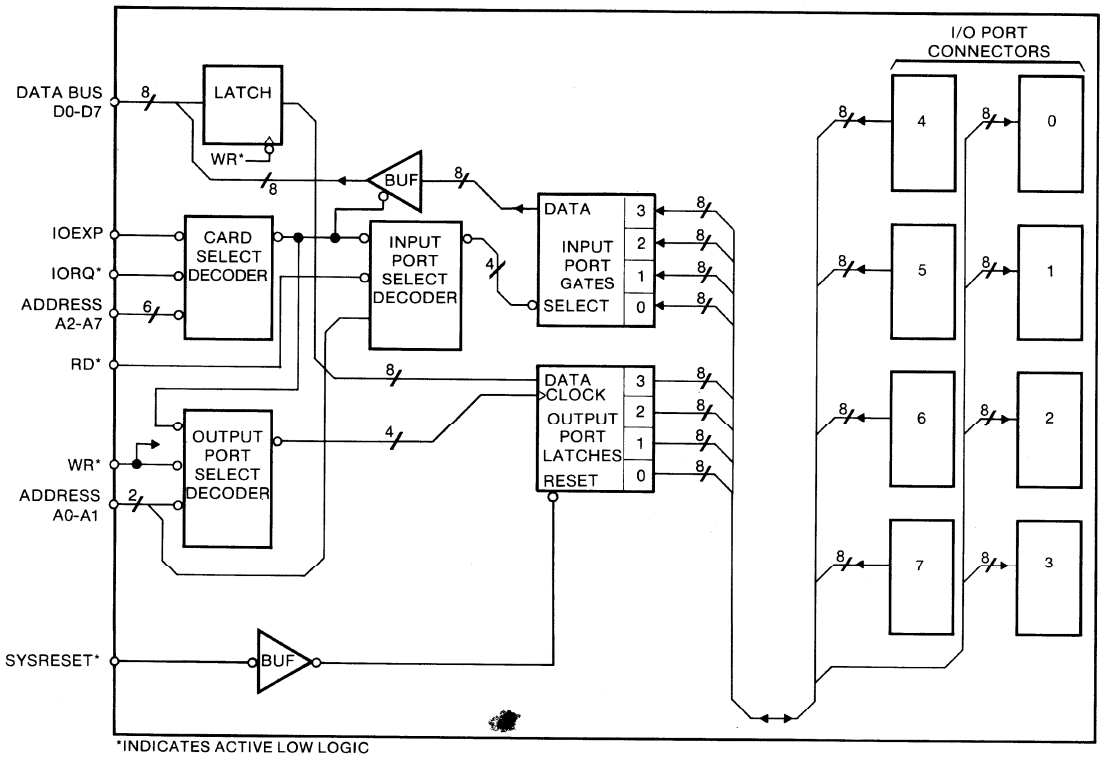


Figure 1-2. Block Diagram (7601A)

INSTALLATION

The 7601A operates as part of an STD BUS card rack system. It must be installed in the card rack with the card ejector toward the top (figure 2-1). A card extender such as the Pro-Log 7901 card can be used to access the 7601A for testing and troubleshooting. Cabling instructions for the 16-pin DIP sockets are given on page 2-4.

CAUTION

To prevent possible damage to your STD BUS system make sure power is **off** before inserting a card into the card rack or removing a card from the card rack.

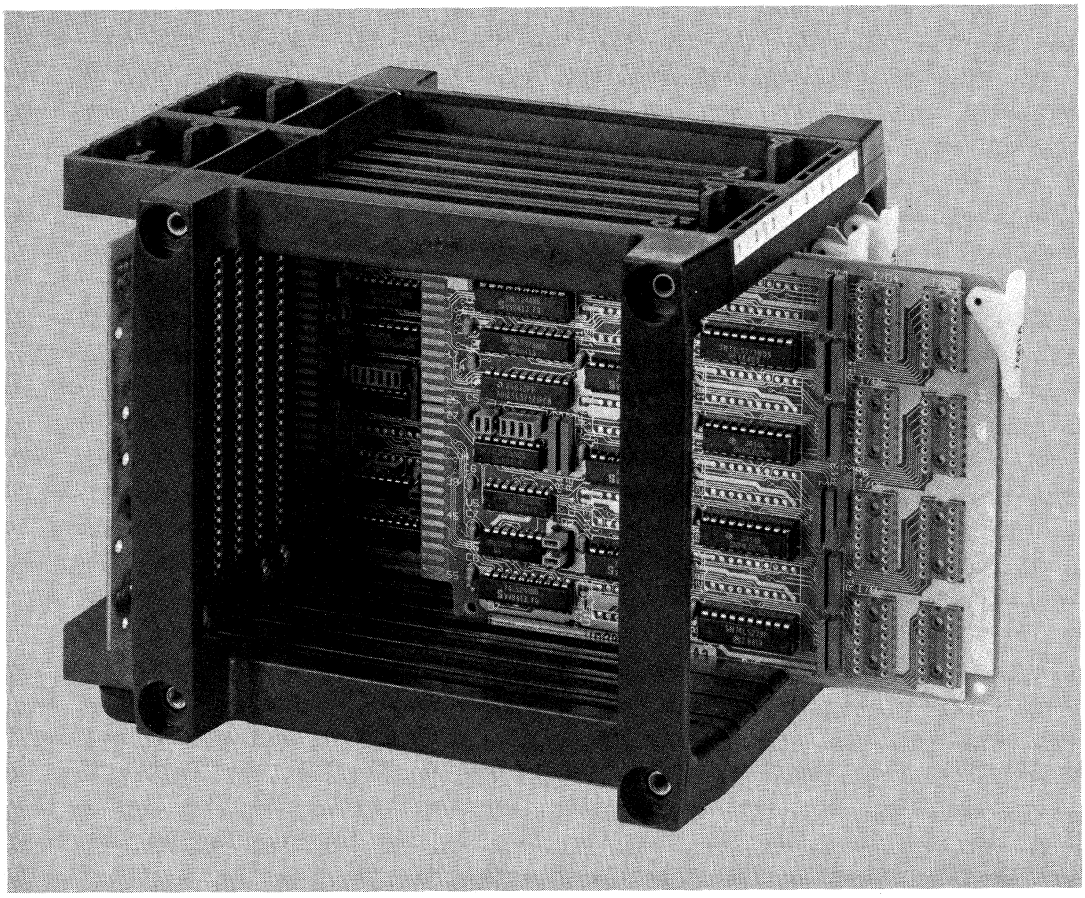


Figure 2-1. Installation (7601A)

I/O MAPPED CARD ADDRESSING

In normal operation, the 7601A is addressed directly by the processor card. The 7601A input and output ports respond to single read and write instructions executed in the processor operating program. The 7601A is enabled when a jumper-selected combination of address lines A0 through A7 is present and when control lines IORQ*, IOEXP, and either RD* or WR* are active.

The 7601A occupies four consecutive I/O addresses regardless of its mapping assignment. The card is shipped with the four ports mapped to addresses 00-03. You may retain these addresses or change them by moving the installed jumpers in the W1 header. While the card's port addresses are generally arbitrary, they must differ from all other I/O port addresses in the system. If they do not differ, multiple cards will respond to the same I/O READ instruction, resulting in BUS contention.

CHANGING THE PORT ADDRESS

The 7601A can be remapped anywhere within the 256-port addressing range of most processors. To change the I/O addressing of the 7601A, move the jumpers in the W1 header. Figure 2-2 shows the W1 header location and jumper installations as shipped. Figure 2-3 shows the jumper positions required for alternate mapping. Note that the jumpers in W2 must remain as shipped for the 7601A to function properly.

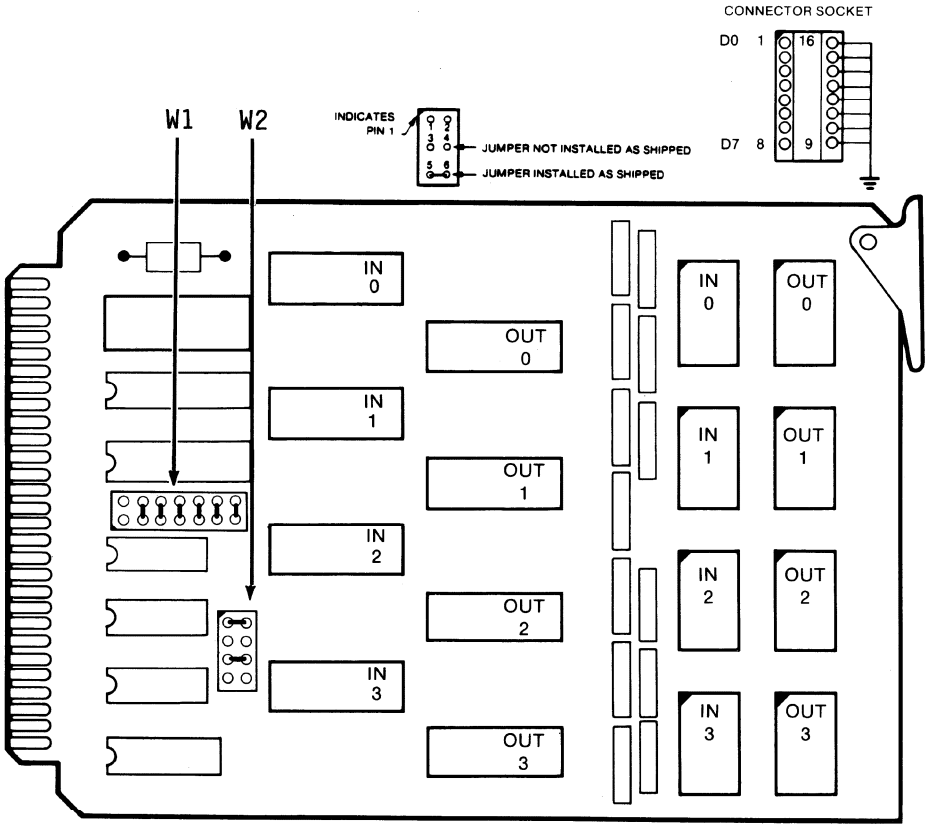


Figure 2-2. Location of Features (7601A)

IOEXP

IOEXP is the I/O expansion line of the STD BUS which allows a system to access 512 I/O ports rather than the standard 256 I/O ports. As shipped, the 7601A is enabled with IOEXP in the low state. Pro-Log processor cards typically connect the IOEXP line to ground. The 7601A can be enabled with IOEXP high by removing jumper W1, 7-8.

ADDRESS RANGE	W1 1-2	3-4	5-6	7-8	9-10	11-12	13-14
00 — 03	●	●	●		●	●	●
04 — 07		●	●		●	●	●
08 — 0B	●		●		●	●	●
0C — 0F			●		●	●	●
10 — 13	●	●			●	●	●
14 — 17		●			●	●	●
18 — 1B	●				●	●	●
1C — 1F					●	●	●
20 — 23	●	●	●		●	●	
24 — 27		●	●		●	●	
28 — 2B	●		●		●	●	
2C — 2F			●		●	●	
30 — 33	●	●		S	●	●	
34 — 37		●		E	●	●	
38 — 3B	●			E	●	●	
3C — 3F					●	●	
40 — 43	●	●	●	N	●		●
44 — 47		●	●	O	●		●
48 — 4B	●		●	T	●		●
4C — 4F			●	E	●		●
50 — 53	●	●			●		●
54 — 57		●		1	●		●
58 — 5B	●				●		●
5C — 5F					●		●
60 — 63	●	●	●		●		
64 — 67		●	●		●		
68 — 6B	●		●		●		
6C — 6F			●		●		
70 — 73	●	●			●		
74 — 77		●			●		
78 — 7B	●				●		
7C — 7F					●		
80 — 83	●	●	●			●	●
84 — 87		●	●			●	●
88 — 8B	●		●			●	●
8C — 8F			●			●	●
90 — 93	●	●				●	●
94 — 97		●				●	●
98 — 9B	●					●	●
9C — 9F						●	●
A0 — A3	●	●	●			●	
A4 — A7		●	●			●	
A8 — AB	●		●			●	
AC — AF			●			●	
B0 — B3	●	●				●	
B4 — B7		●				●	
B8 — BB	●					●	
BC — BF						●	
C0 — C3	●	●	●				●
C4 — C7		●	●				●
C8 — CB	●		●				●
CC — CF			●				●
D0 — D3	●	●					●
D4 — D7		●					●
D8 — DB	●						●
DC — DF							●
E0 — E3	●	●	●				
E4 — E7		●	●				
E8 — EB	●		●				
EC — EF			●				
F0 — F3	●	●					
F4 — F7		●					
F8 — FB	●						
FC — FF							

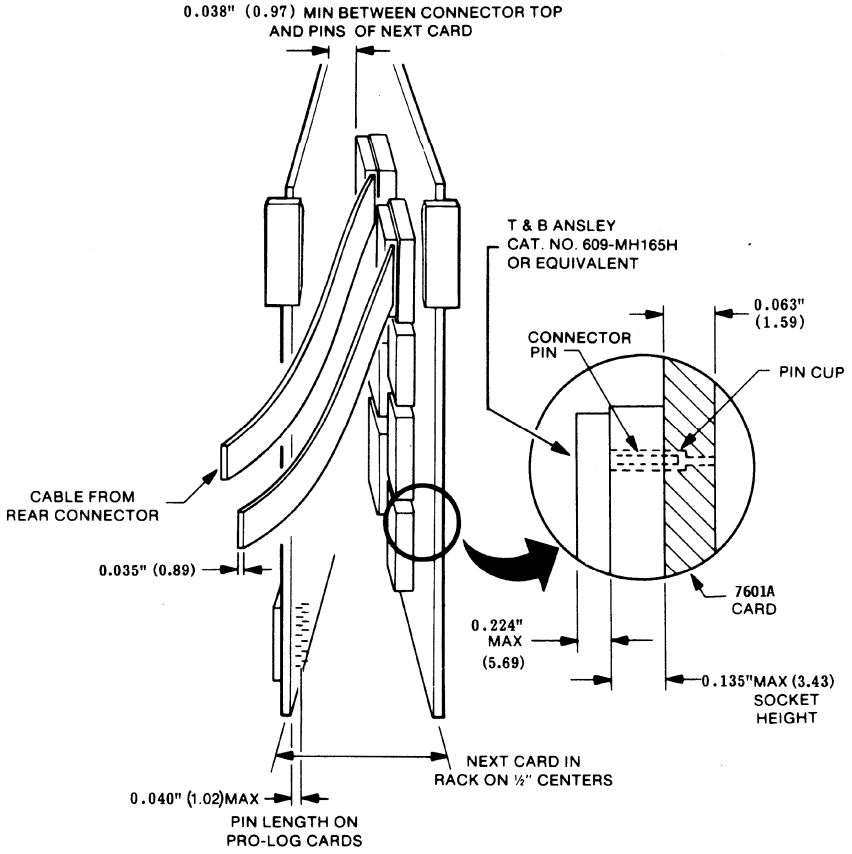
NOTES:
1. For explanation of Jumper W1; 7-8 refer to the "IOEXP" heading.
2. Dot ● indicates jumper installed.
3. Jumpers W2, 1-2 and 5-6 installed, 3-4 and 7-8 not installed.

Figure 2-3. Address Selection Jumpers (7601A)

CABLING

Figure 2-2 (page 2-2) shows the connector associated with each port and the relation of pins to data lines. If the cards are on 1/2-inch centers, use a low-profile connector (figure 2-4). This allows the cable from the rear set of plugs to pass over the outer set. A low-profile connector is suggested, such as T and B Ansley Catalog part number 609-MH165H or equivalent. The connectors should have gold-plated pins to take full advantage of the noncorrosive, high-contact ability provided by the gold-plated contacts in the sockets. The connectors have a high retention rate, preventing the plugs from working loose under normal conditions.

The distance a cable can be extended depends upon the environment. Drive and load characteristics of the I/O latches and buffers are given at the end of this section. Using alternating ground lines helps reduce noise sensitivity.


0.038" (0.97) MIN BETWEEN CONNECTOR TOP AND PINS OF NEXT CARD
T & B ANSLEY CAT. NO. 609-MH165H OR EQUIVALENT
0.063" (1.59)
CONNECTOR PIN
PIN CUP
CABLE FROM REAR CONNECTOR
0.035" (0.89)
7601A CARD
0.224" MAX (5.69)
0.135"MAX (3.43) SOCKET HEIGHT
NEXT CARD IN RACK ON ½" CENTERS
0.040" (1.02)MAX
PIN LENGTH ON PRO-LOG CARDS

Dimensions in millimeters shown in parentheses.

Figure 2-4. Low-Profile Connector (7601A)

TIONS

meets all mechanical specifications of the STD BUS. For information and suggested connectors refer to Cabling, page 2-4.

and Environmental

JS.

TER	RECOMMENDED OPERATING LIMITS			ABSOLUTE NONOPERATING LIMITS		
	MIN	TYP	MAX	MIN	MAX	UNITS
)	0	+25	+65	-40	+75	°C
Relative	5	—	95	5	95	%RH
e	4.75	5.00	5.25	0	5.50	V
t	—	364	576	—	—	mA

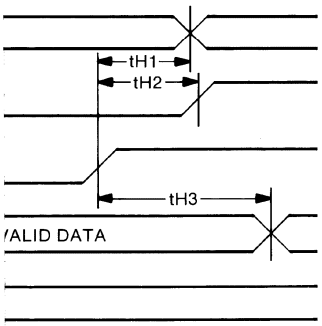


Figure 2-5. Electrical and Environmental Specifications (7601A)

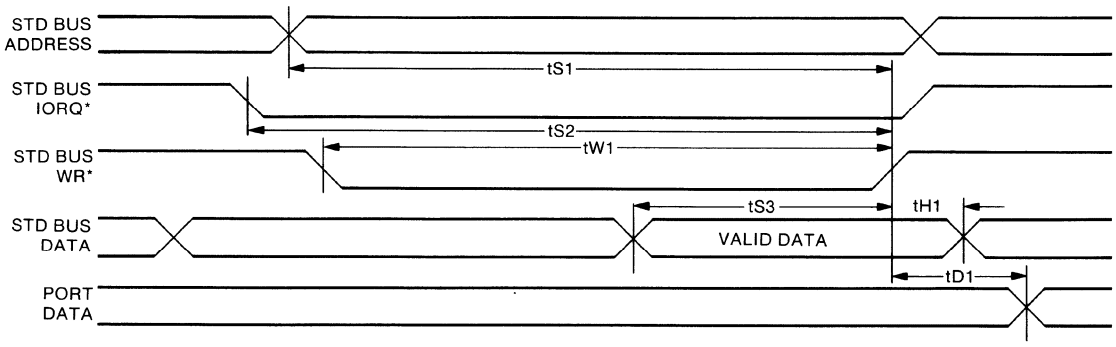
	NANOSECONDS	
	MIN	MAX
		150
		125
		130
	40	
	45	
	90	
	45	

nterface

2-6 for the 7601A-to-STD BUS interface specifications.

face

evel: TTL
ive: 16 LSTTL loads
l: 4 LSTTL loads
eresis: 0.2V minimum
0.4V typical



SYMBOL	PARAMETER	NANOSECONDS	
		MIN	MAX
tD1	Port data delay from WR* inactive		85
tH1	Data hold after WR* inactive	45	
tS1	Address setup before WR* inactive	85	
tS2	IORQ* setup before WR* inactive	100	
tS3	Data setup before WR* inactive	40	
tW1	WR* pulse width	75	

Figure 2-8. Write Timing (7601A)

OPERATION

To operate the 7601A I/O card, simply write to or read from the desired port. The data is not inverted. The output latches are two-state.

Section 4

OPERATING SOFTWARE

Section 4 is normally reserved for software. The 7601A requires no special software.

REFERENCE DRAWINGS

The schematic (figure 5-1) and assembly drawing (figure 5-2) in the following pages are included in this manual FOR REFERENCE USE ONLY. These drawings may differ in some respects from the card you receive from Pro-Log. If you require the specific revision documents of the schematic and assembly for the board shipped, please use the information request form in the back of this manual to order them.

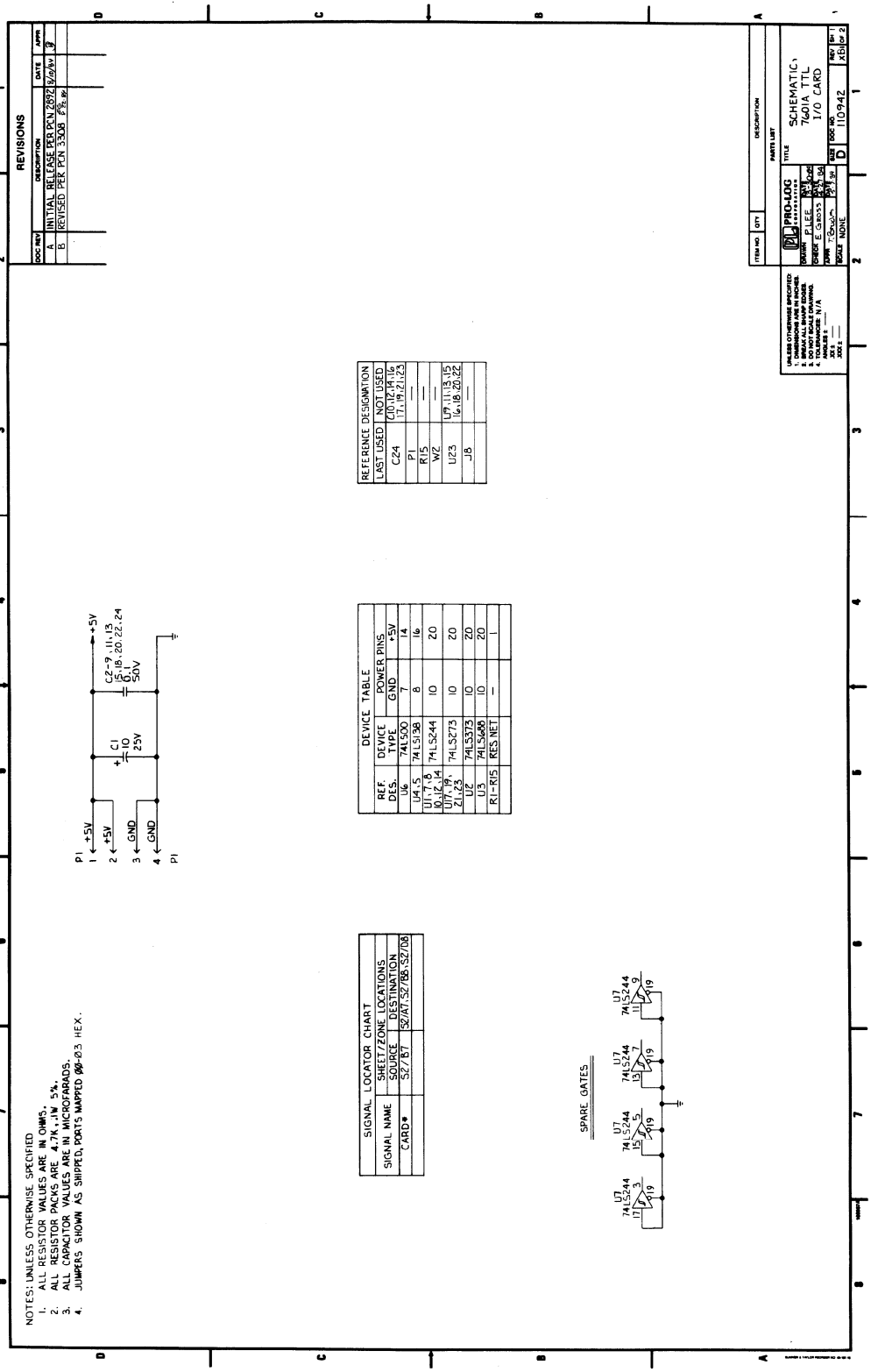


Figure 5-1. Schematic (7601A)
(FOR REFERENCE ONLY)

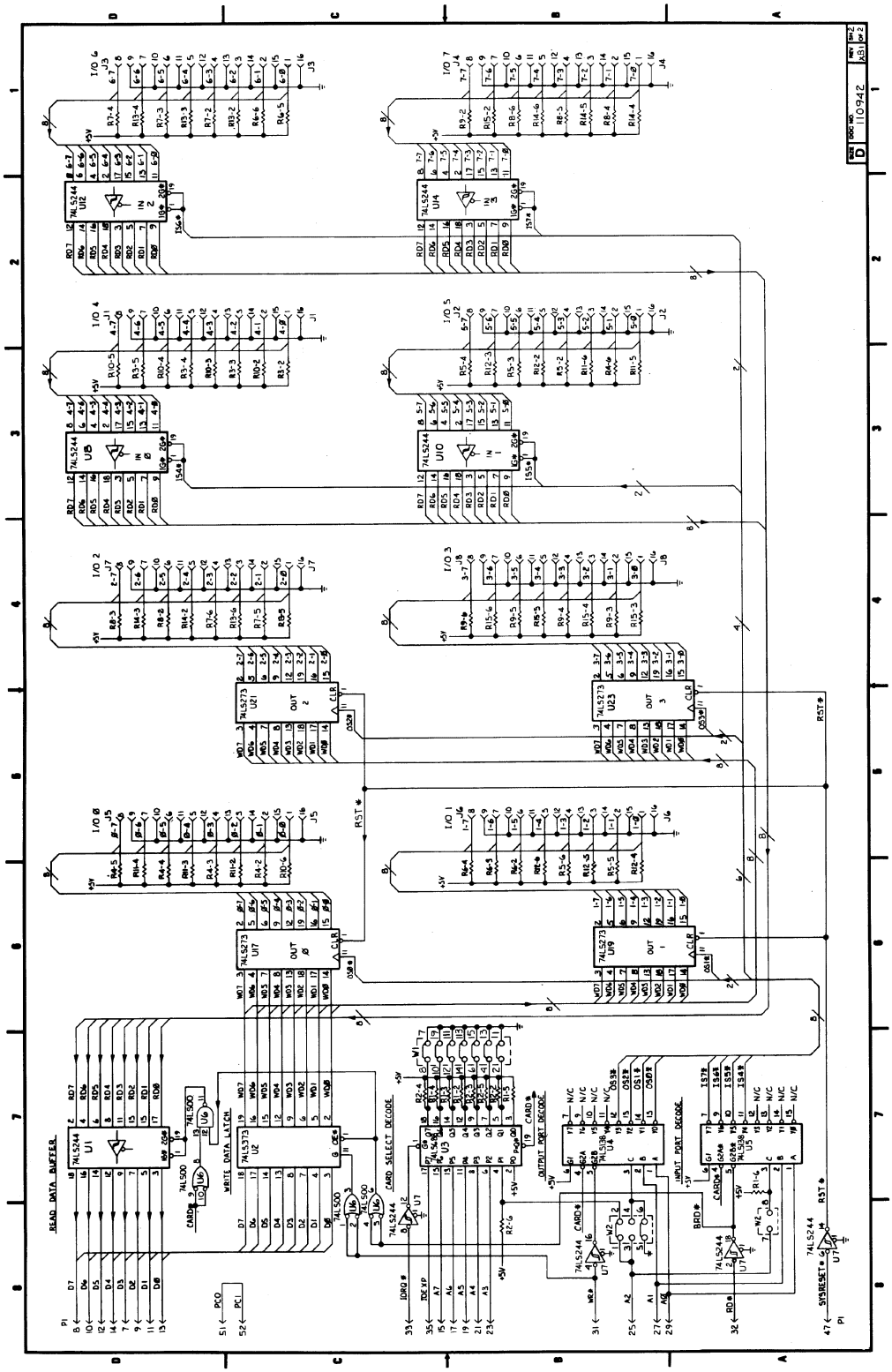
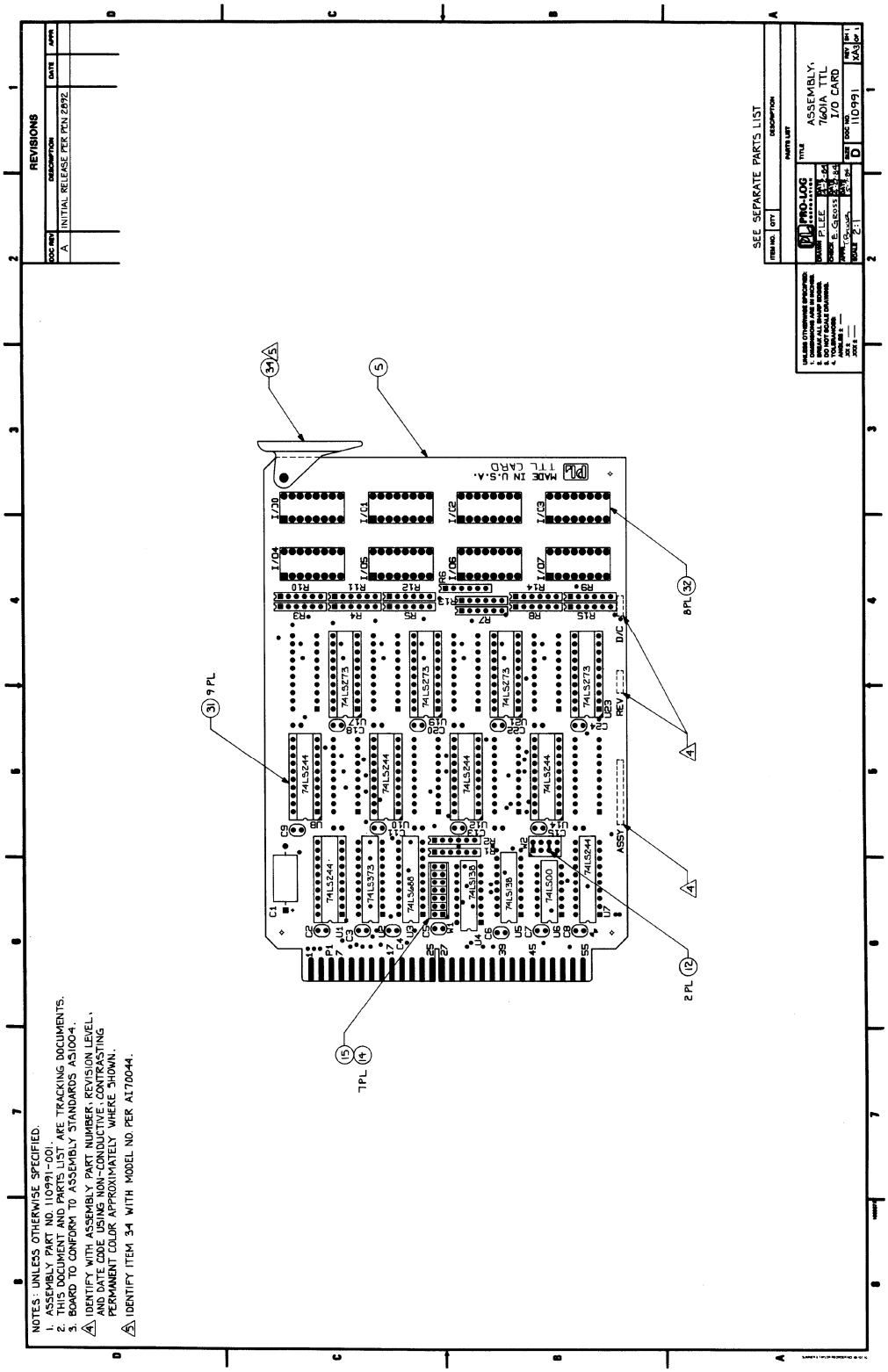


Figure 5-1. Schematic (7601A) Continued
(FOR REFERENCE ONLY)


REVISIONS
DESCRIPTION
INITIAL RELEASE PER PCN 2892
NOTES: UNLESS OTHERWISE SPECIFIED.
1. ASSEMBLY PART NO. 110991-001.
2. THIS DOCUMENT AND PARTS LIST ARE TRACKING DOCUMENTS.
3. BOARD TO CONFORM TO ASSEMBLY STANDARDS A51004.
4. IDENTIFY WITH ASSEMBLY PART NUMBER, REVISION LEVEL, AND DATE CODE USING NON-CONDUCTIVE, CONTRASTING PERMANENT COLOR APPROXIMATELY WHERE SHOWN.
5. IDENTIFY ITEM 34 WITH MODEL NO. PER A1-7004.
SEE SEPARATE PARTS LIST
ASSEMBLY: 7601A TTL I/O CARD
DOC NO. 110991
MADE IN U.S.A.
TTL CARD
74LS244
74LS273
74LS373
74LS368
74LS138
74LS00
74LS32
74LS86
74LS38
74LS74
74LS123
74LS04
74LS08
74LS10
74LS20
74LS30
74LS51
74LS54
74LS86
74LS109
74LS112
74LS125
74LS132
74LS133
74LS136
74LS139
74LS151
74LS153
74LS157
74LS158
74LS161
74LS163
74LS164
74LS165
74LS166
74LS174
74LS175
74LS181
74LS182
74LS190
74LS191
74LS192
74LS193
74LS194
74LS195
74LS196
74LS197
74LS221
74LS240
74LS241
74LS242
74LS243
74LS245
74LS247
74LS248
74LS249
74LS251
74LS253
74LS257
74LS258
74LS259
74LS260
74LS261
74LS266
74LS273
74LS279
74LS280
74LS283
74LS290
74LS293
74LS295
74LS298
74LS299
74LS322
74LS323
74LS324
74LS325
74LS326
74LS327
74LS328
74LS329
74LS330
74LS331
74LS332
74LS333
74LS334
74LS335
74LS336
74LS337
74LS338
74LS339
74LS340
74LS341
74LS342
74LS343
74LS344
74LS345
74LS346
74LS347
74LS348
74LS349
74LS350
74LS351
74LS352
74LS353
74LS354
74LS355
74LS356
74LS357
74LS358
74LS359
74LS360
74LS361

STD 7000

7602A

TTL Output Card

USER'S MANUAL

CONTENTS

	Page
Figures	iv
Section 1 - Purpose and Main Features	1-1
Purpose	1-1
Features	1-1
Section 2 - Installation and Specifications	2-1
Installation	2-1
I/O Mapped Card Addressing	2-2
Changing the Port Address	2-2
IOEXP	2-3
Cabling	2-4
Specifications	2-5
STD BUS Interface	2-5
Port Interface	2-5
Timing	2-7
Section 3 - Operation and Programming	3-1
Operation	3-1
Section 4 - Operating Software	4-1
Section 5 - Maintenance	5-1
Reference Drawings	5-1

FIGURES

Figure		Page
1-1	7602A	1-1
1-2	Block Diagram	1-2
2-1	Installation	2-1
2-2	Location of Features	2-2
2-3	Address Selection Jumpers	2-3
2-4	Low-Profile Connector	2-4
2-5	Electrical and Environmental Specifications	2-5
2-6	7602A/STD BUS Interface Specifications	2-6
2-7	Write Timing	2-7
5-1	Schematic	5-2
5-2	Assembly	5-4

PURPOSE

The 7602A provides eight 8-bit TTL latched output ports, 64 lines total. The output lines can drive 16 LSTTL loads (4 TTL loads). The card decodes eight address lines and the STD BUS IOEXP signal. Slip-on connectors allow mapping to any consecutive group of eight addresses. The STD BUS SYSRESET* signal clears all output ports simultaneously.

FEATURES

- Eight 8-bit output ports, 64 lines
- Outputs drive 16 LSTTL loads (4 TTL loads)
- Occupies eight consecutive addresses
- Flexible I/O mapping
- +5V operation
- Universal processor compatibility

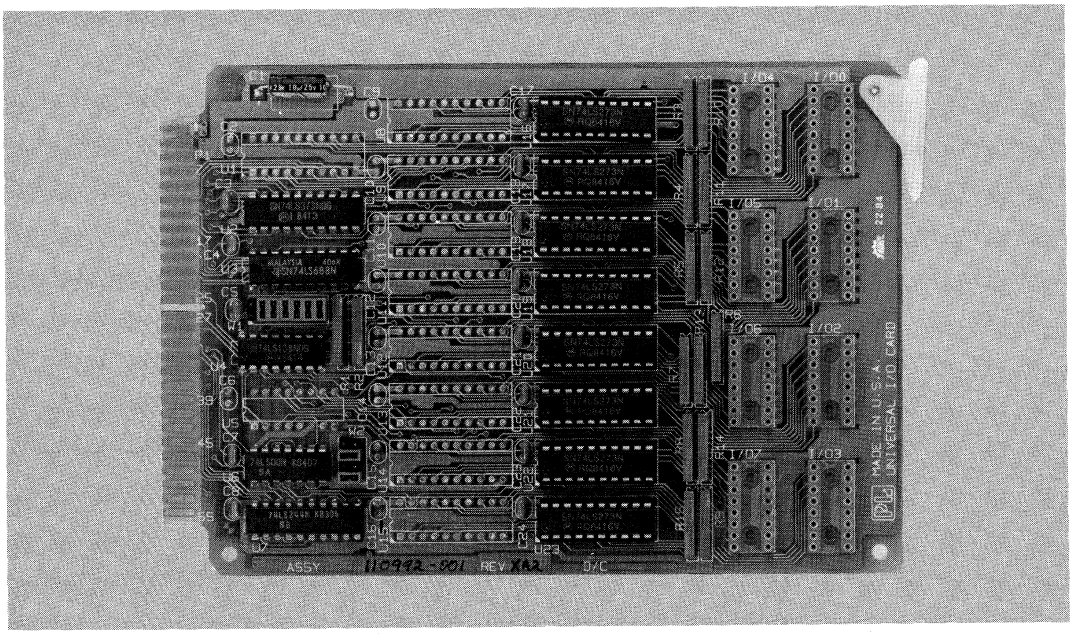


Figure 1-1. 7602A

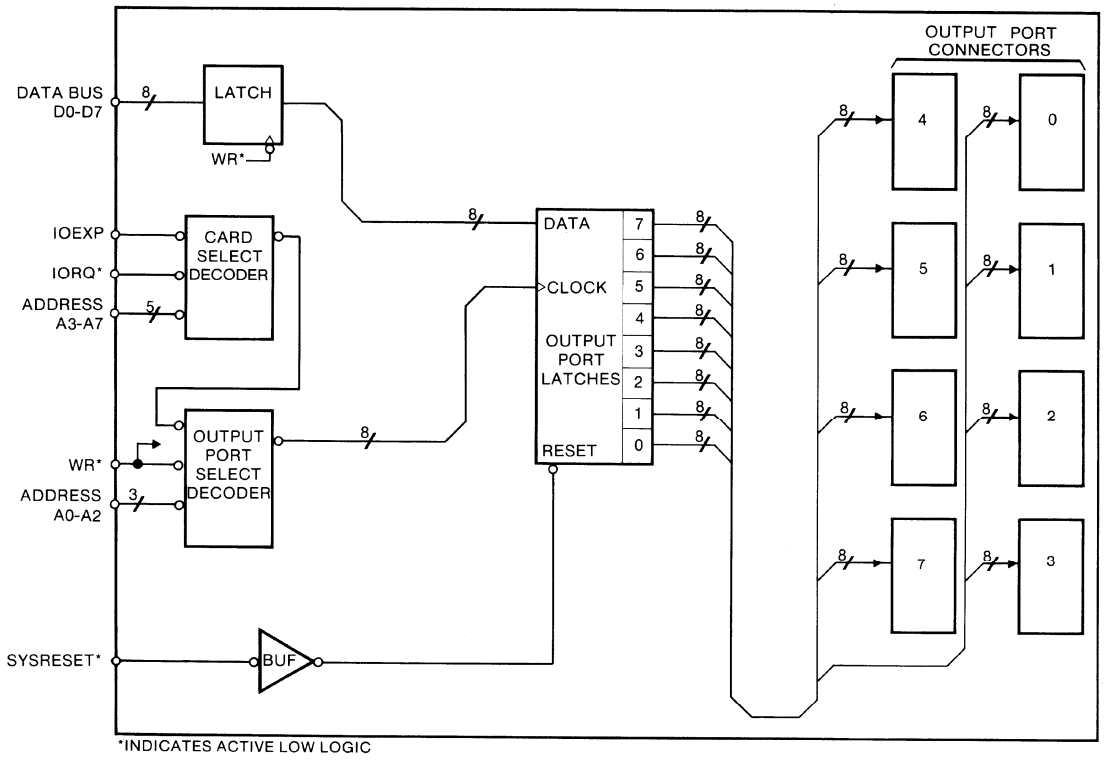


Figure 1-2. Block Diagram (7602A)

INSTALLATION

The 7602A operates as part of an STD BUS card rack system. It must be installed in the card rack with the card ejector toward the top (figure 2-1). A card extender such as the Pro-Log 7901 card can be used to access the 7602A for testing and troubleshooting. Cabling instructions for the 16-pin DIP sockets are given on page 2-4.

CAUTION

To prevent possible damage to your STD BUS system make sure power is **off** before inserting a card into the card rack or removing a card from the card rack.

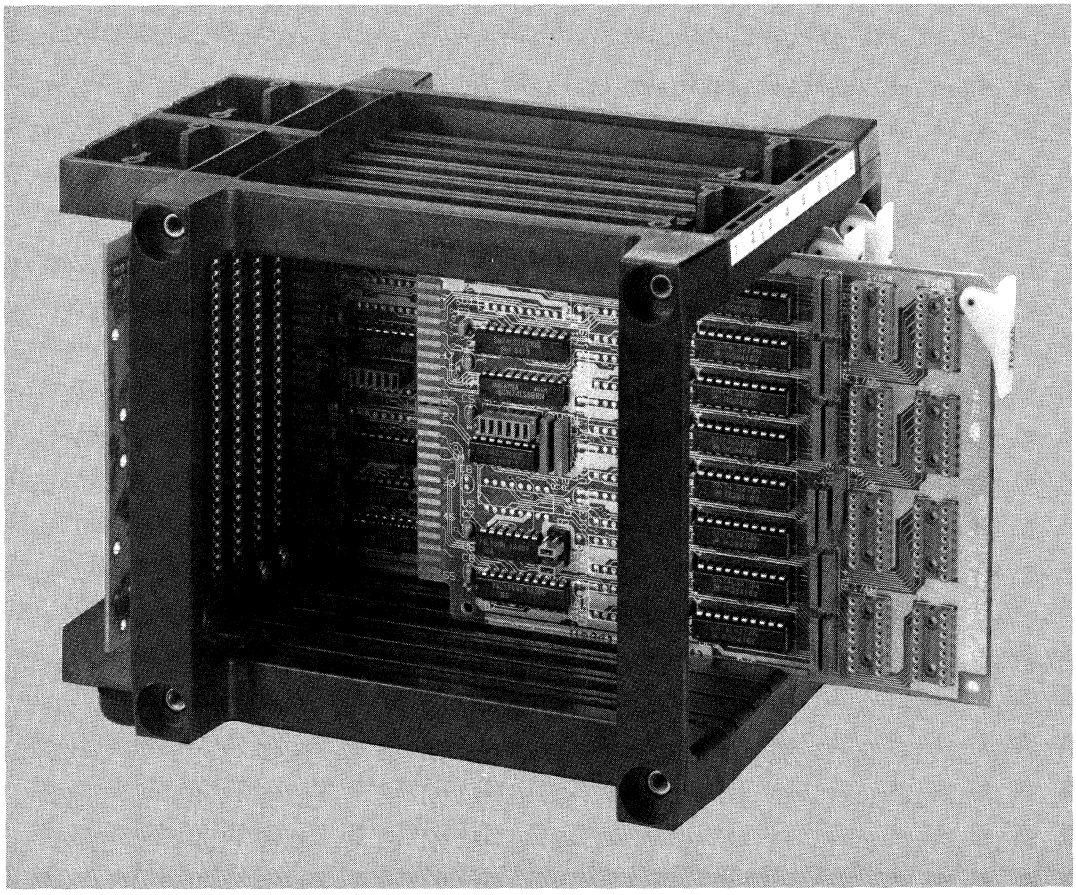


Figure 2-1. Installation (7602A)

I/O MAPPED CARD ADDRESSING

In normal operation, the 7602A is addressed directly by the processor card. The 7602A output ports respond to single write instructions executed in the processor operating program. The 7602A is enabled when a jumper-selected combination of address lines A0 through A7 is present and when control lines IORQ*, IOEXP, and WR* are active.

The 7602A occupies eight consecutive I/O addresses regardless of its mapping assignment. The card is shipped with the eight ports mapped to addresses 00-07. You may retain these addresses or change them by moving the installed jumpers in the W1 header. While the card's port addresses are generally arbitrary, they must differ from all other output port addresses in the system. If they do not differ, multiple cards will respond to the same I/O WRITE instruction. The same eight addresses may be used for input ports.

CHANGING THE PORT ADDRESS

The 7602A can be remapped anywhere within the 256-port addressing range of most processors. To change the I/O addressing of the 7602A, move the jumpers in the W1 header. Figure 2-2 shows the W1 header location and jumper installation as shipped. Figure 2-3 shows the jumper positions required for alternate mapping. Note that the jumpers in W2 must remain as shipped for the 7602A to function properly.

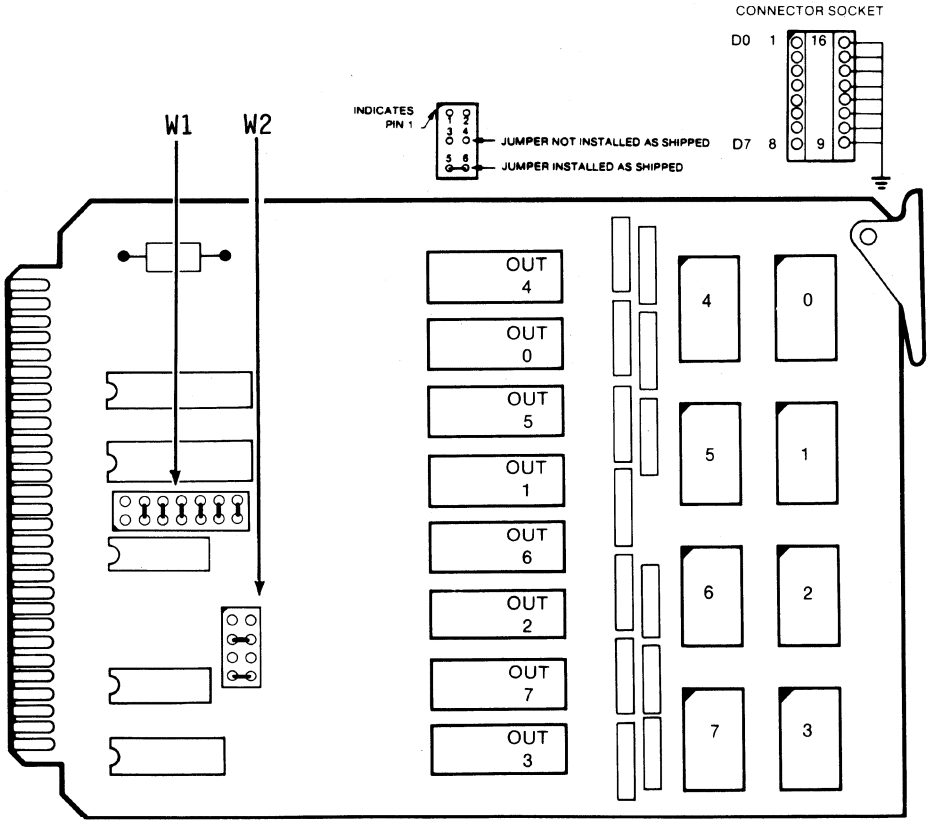


Figure 2-2. Location of Features (7602A)

IOEXP

IOEXP is the I/O expansion line of the STD BUS that allows a system to access 512 I/O ports rather than the standard 256 I/O ports. As shipped, the 7602A is enabled with IOEXP in the low state. Pro-Log processor cards typically connect the IOEXP line to ground. The 7602A can be enabled with IOEXP high by removing jumper W1, 7-8.

ADDRESS RANGE	W1						
	1-2	3-4	5-6	7-8	9-10	11-12	13-14
00 — 07		●	●		●	●	●
08 — 0F			●		●	●	●
10 — 17		●			●	●	●
18 — 1F					●	●	●
20 — 27		●	●		●	●	
28 — 2F			●		●	●	
30 — 37		●			●	●	
38 — 3F					●	●	
40 — 47		●	●		●		●
48 — 4F			●	S	●		●
50 — 57		●		E	●		●
58 — 5F				E	●		●
60 — 67		●	●		●		
68 — 6F			●	N	●		
70 — 77		●		O	●		
78 — 7F				T	●		
80 — 87		●	●	E		●	●
88 — 8F			●			●	●
90 — 97		●		1		●	●
98 — 9F						●	●
A0 — A7		●	●			●	
A8 — AF			●			●	
B0 — B7		●				●	
B8 — BF						●	
C0 — C7		●	●				●
C8 — CF			●				●
D0 — D7		●					●
D8 — DF							●
E0 — E7		●	●				
E8 — EF			●				
F0 — F7		●					
F8 — FF							

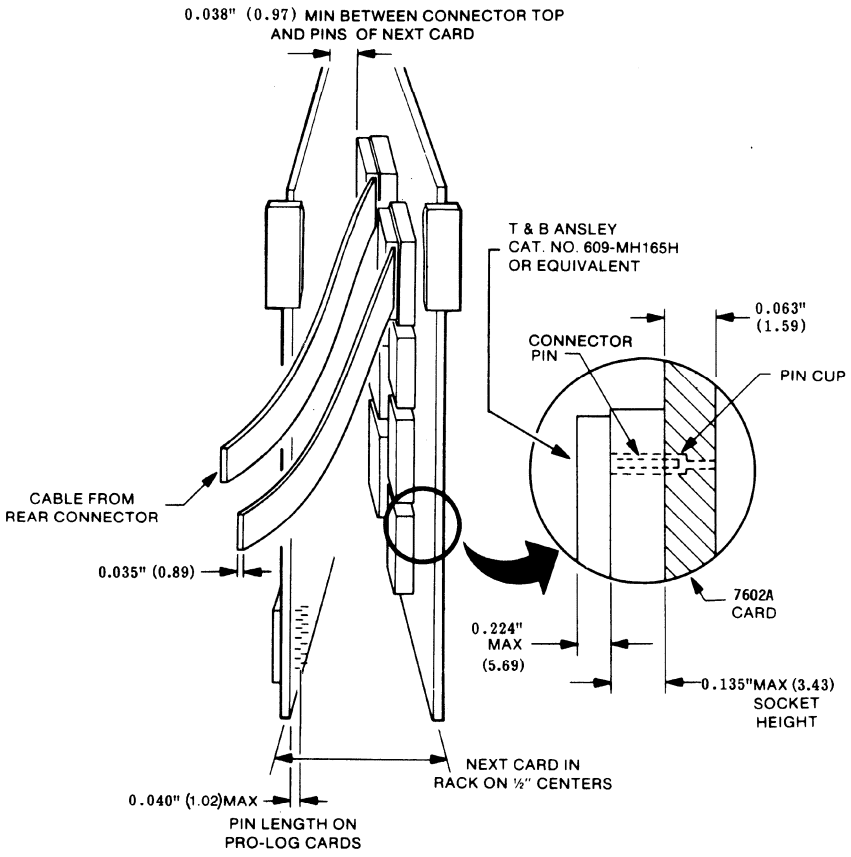
NOTES:
1. For explanation of Jumper W1; 7-8 refer to the "IOEXP" heading.
2. Dot ● indicates jumper installed.
3. Jumpers W2, 3-4 and 7-8 installed.

Figure 2-3. Address Selection Jumpers (7602A)

CABLING

Figure 2-2 (page 2-2) shows the connector associated with each port and the relation of pins to data lines. If the cards are on 1/2-inch centers, use a low-profile connector (figure 2-4). This allows the cable from the rear set of plugs to pass over the outer set. A low-profile connector is suggested, such as T and B Ansley Catalog part number 609-MH165H or equivalent. The connectors should have gold-plated pins to take full advantage of the noncorrosive, high-contact ability provided by the gold-plated contacts in the sockets. The connectors have a high retention rate, preventing the plugs from working loose under normal conditions.

The distance a cable can be extended depends upon the environment. Drive characteristics of the output latches are given at the end of this section. Using alternating ground lines helps reduce noise sensitivity.


0.038" (0.97) MIN BETWEEN CONNECTOR TOP AND PINS OF NEXT CARD
T & B ANSLEY CAT. NO. 609-MH165H OR EQUIVALENT
0.063" (1.59)
CONNECTOR PIN
PIN CUP
CABLE FROM REAR CONNECTOR
0.035" (0.89)
7602A CARD
0.224" MAX (5.69)
0.135"MAX (3.43) SOCKET HEIGHT
NEXT CARD IN RACK ON ½" CENTERS
0.040" (1.02)MAX
PIN LENGTH ON PRO-LOG CARDS

Dimensions in millimeters shown in parentheses.

Figure 2-4. Low-Profile Connector (7602A)

SPECIFICATIONS

Mechanical

The 7602A meets all mechanical specifications of the STD BUS. For information on cabling and suggested connectors refer to Cabling, page 2-4.

Electrical and Environmental

	RECOMMENDED OPERATING LIMITS			ABSOLUTE NONOPERATING LIMITS		
PARAMETER	MIN	TYP	MAX	MIN	MAX	UNITS
Free Air Temp	0	+25	+65	-40	+75	°C
Noncondensing Relative Humidity	5	—	95	5	95	%RH
Supply Voltage	4.75	5.00	5.25	0	5.50	V
Supply Current	—	272	414	—	—	mA

Figure 2-5. Electrical and Environmental Specifications (7602A)

STD BUS Interface

See figure 2-6 for the 7602A-to-STD BUS interface specifications.

Port Interface

Voltage Level: TTL
Output Drive: 16 LSTTL loads

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
2	IN		+5V	1		IN	+5V
4	IN		GROUND	3		IN	GROUND
6			-5V	5			-5V
8	1		D7	7		1	D3
10	1		D6	9		1	D2
12	1		D5	11		1	D1
14	1		D4	13		1	D0
16			A15	15		1	A7
18			A14	17		1	A6
20			A13	19		1	A5
22			A12	21		1	A4
24			A11	23		1	A3
26			A10	25		3	A2
28			A9	27		1	A1
30			A8	29		1	A0
32	1		RD*	31		3	WR*
34			MEMRQ*	33		1	IORQ*
36			MEMEX	35		1	IOEXP
38			MCSYNC*	37			REFRESH*
40			STATUS 0*	39			STATUS 1*
42			BUSRQ*	41			BUSAK*
44			INTRQ*	43			INTAK*
46			NMIRQ*	45			WAITRQ*
48			PBRESET*	47		1	SYSRESET*
50			CNTRL*	49			CLOCK*
52	IN		PCI	51	OUT		PCO
54			AUX GND	53			AUX GND
56			AUX -V	55			AUX +V

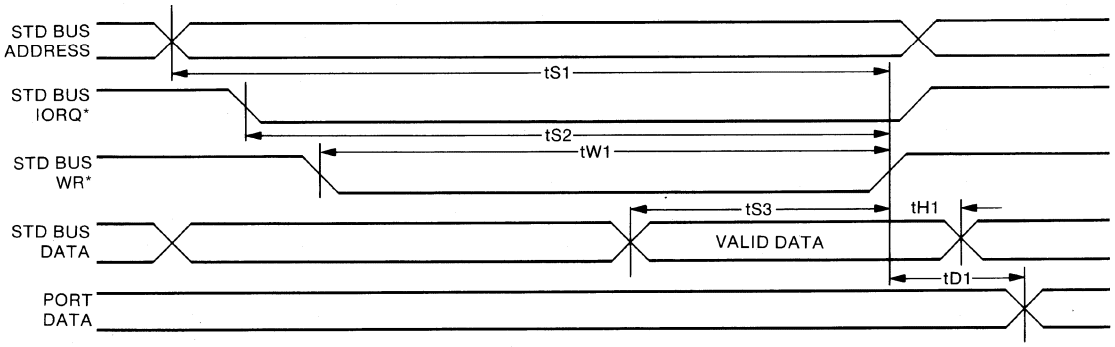
* Designates active low-level logic

Figure 2-6. 7602A/STD BUS Interface Specifications

Timing

Timing data is specified at the following conditions:

V_{CC}:	4.75 to 5.25V
T:	0 to 65°C
Capacitive Load:	15 pf on output ports, 45 pf on STD BUS.



SYMBOL	PARAMETER	NANOSECONDS MIN	NANOSECONDS MAX
tD1	Port data delay from WR* inactive		85
tH1	Data hold after WR* inactive	45	
tS1	Address setup before WR* inactive	85	
tS2	IORQ* setup before WR* inactive	100	
tS3	Data setup before WR* inactive	40	
tW1	WR* pulse width	75	

Figure 2-7. Write Timing (7602A)

Section 3

OPERATION AND PROGRAMMING

OPERATION

To operate the 7602A output card, simply write to the desired port. The data is not inverted. The output latches are two-state.

Section 4

OPERATING SOFTWARE

Section 4 is normally reserved for software. The 7602A requires no special software.

REFERENCE DRAWINGS

The schematic (figure 5-1) and assembly drawing (figure 5-2) in the following pages are included in this manual FOR REFERENCE USE ONLY. These drawings may differ in some respects from the card you receive from Pro-Log. If you require the specific revision documents of the schematic and assembly for the board shipped, please use the information request form in the back of this manual to order them.

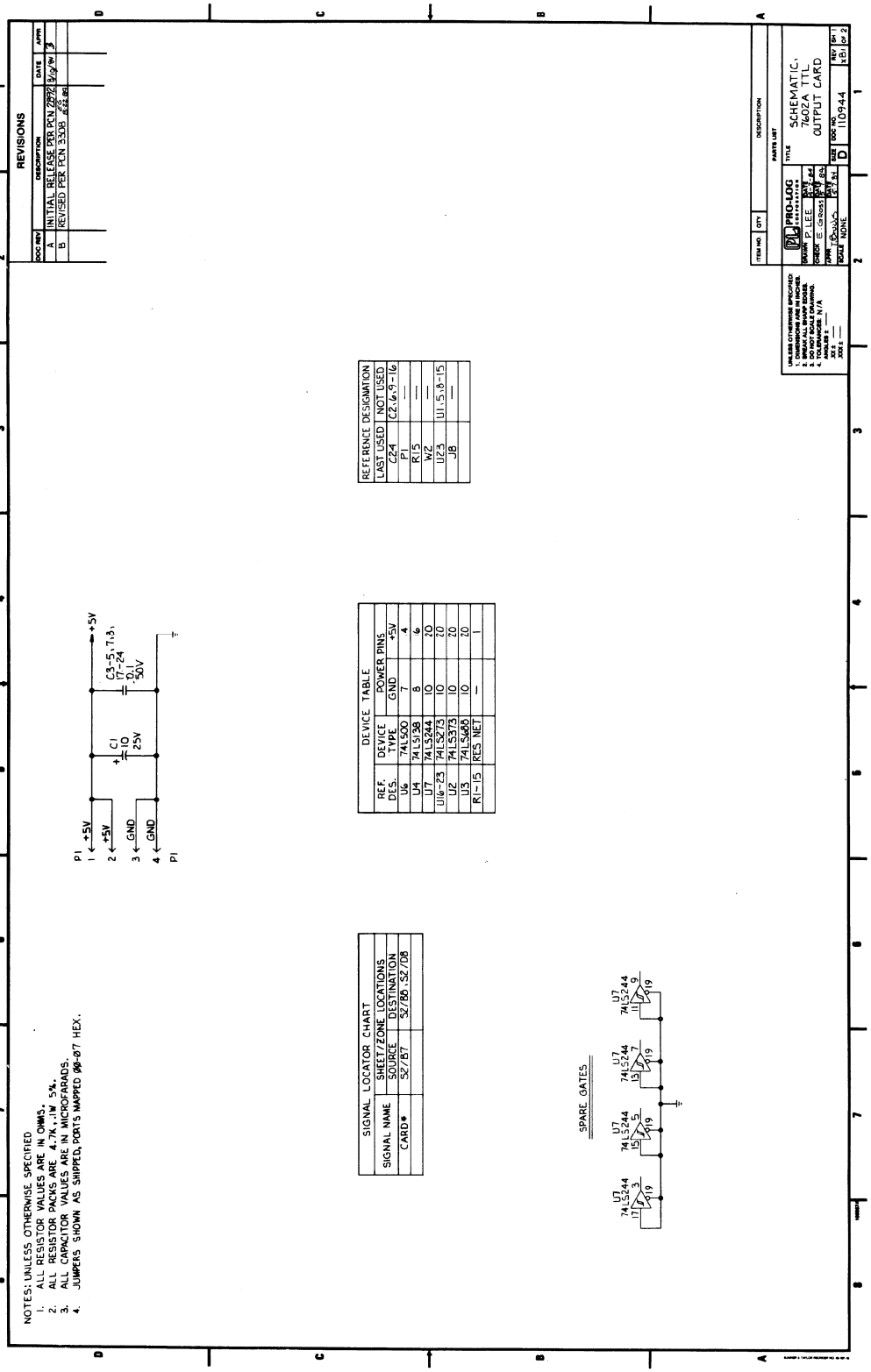

REVISIONS
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS.
2. ALL RESISTOR PACKS ARE 4.7K, 1W 5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. JUMPERS SHOWN AS SHIPPED, PORTS MAPPED 00-07 HEX.
SIGNAL LOCATOR CHART
DEVICE TABLE
REFERENCE DESIGNATION
SPARE GATES
SCHEMATIC, 7602A TTL OUTPUT CARD
PRO-LOG

Figure 5-1. Schematic (7602A)
(FOR REFERENCE ONLY)

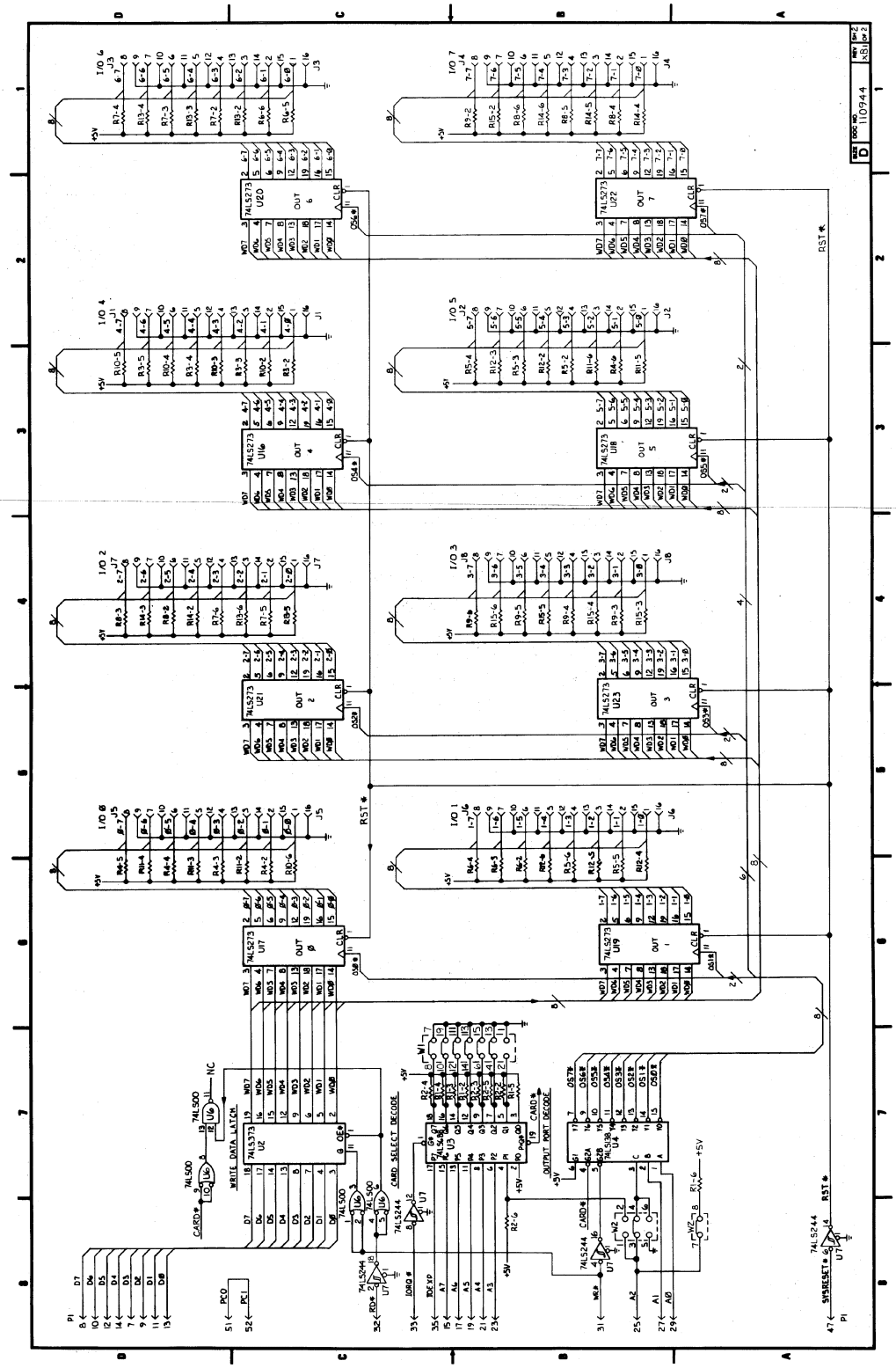


Figure 5-1. Schematic (7602A) Continued
(FOR REFERENCE ONLY)

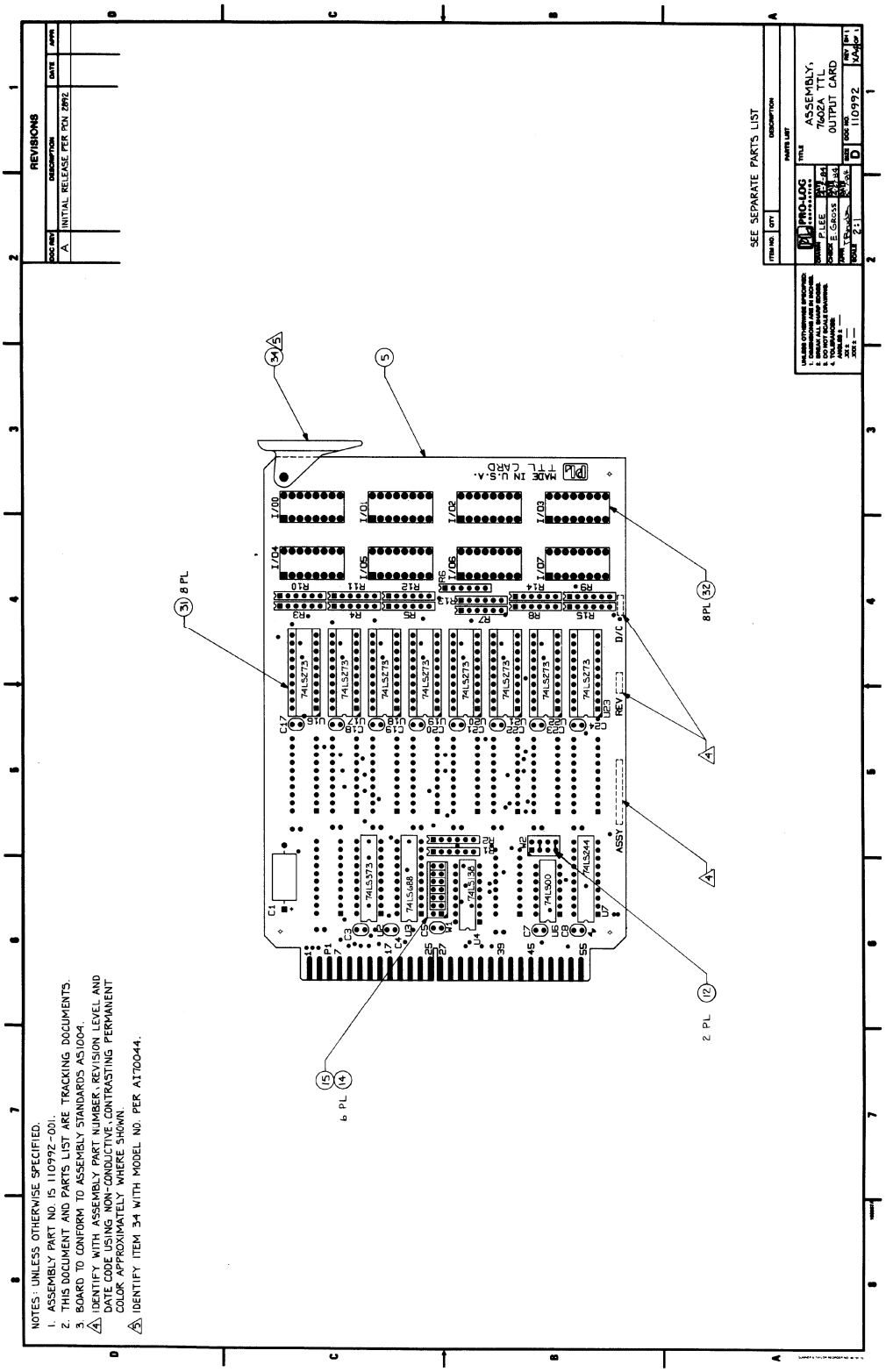


Figure 5-2. Assembly (7602A)
(FOR REFERENCE ONLY)

STD 7000

7603A

TTL Input Card

USER'S MANUAL

CONTENTS

	Page
Figures	iv
Section 1 - Purpose and Main Features	1-1
Purpose	1-1
Features	1-1
Section 2 - Installation and Specifications	2-1
Installation	2-1
I/O Mapped Card Addressing	2-2
Changing the Port Address	2-2
IOEXP	2-3
Cabling	2-4
Specifications	2-5
STD BUS Interface	2-5
Port Interface	2-5
Timing	2-7
Section 3 - Operation and Programming	3-1
Operation	3-1
Section 4 - Operating Software	4-1
Section 5 - Maintenance	5-1
Reference Drawings	5-1

FIGURES

Figure		Page
1-1	7603A	1-1
1-2	Block Diagram	1-2
2-1	Installation	2-1
2-2	Location of Features	2-2
2-3	Address Selection Jumpers	2-3
2-4	Low-Profile Connector	2-4
2-5	Electrical and Environmental Specifications	2-5
2-6	7603A/STD BUS Interface Specifications	2-6
2-7	Read Timing	2-7
5-1	Schematic	5-2
5-2	Assembly	5-4

PURPOSE

The 7603A provides eight 8-bit TTL buffered input ports, 64 lines total. The input lines are noninverting. The card decodes eight address lines and the STD BUS IOEXP signal. Slip-on connectors allow mapping to any consecutive group of eight addresses.

FEATURES

- Eight 8-bit input ports, 64 lines
- Inputs present 4 LSTTL loads (1 TTL load)
- Occupies eight consecutive I/O addresses
- Flexible I/O mapping
- +5V operation
- Universal processor compatibility

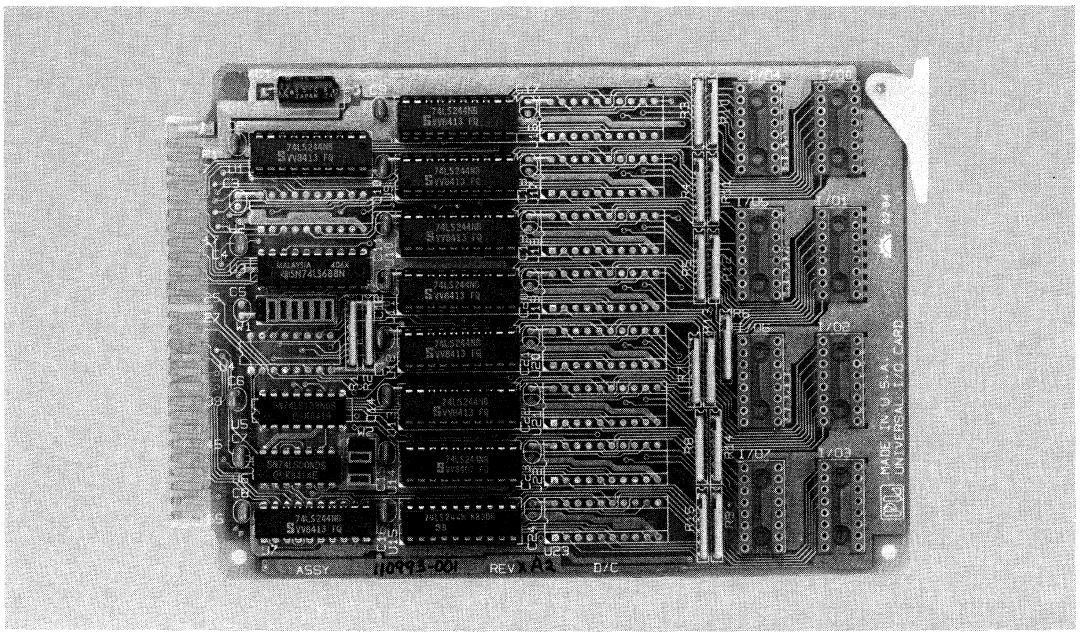


Figure 1-1. 7603A

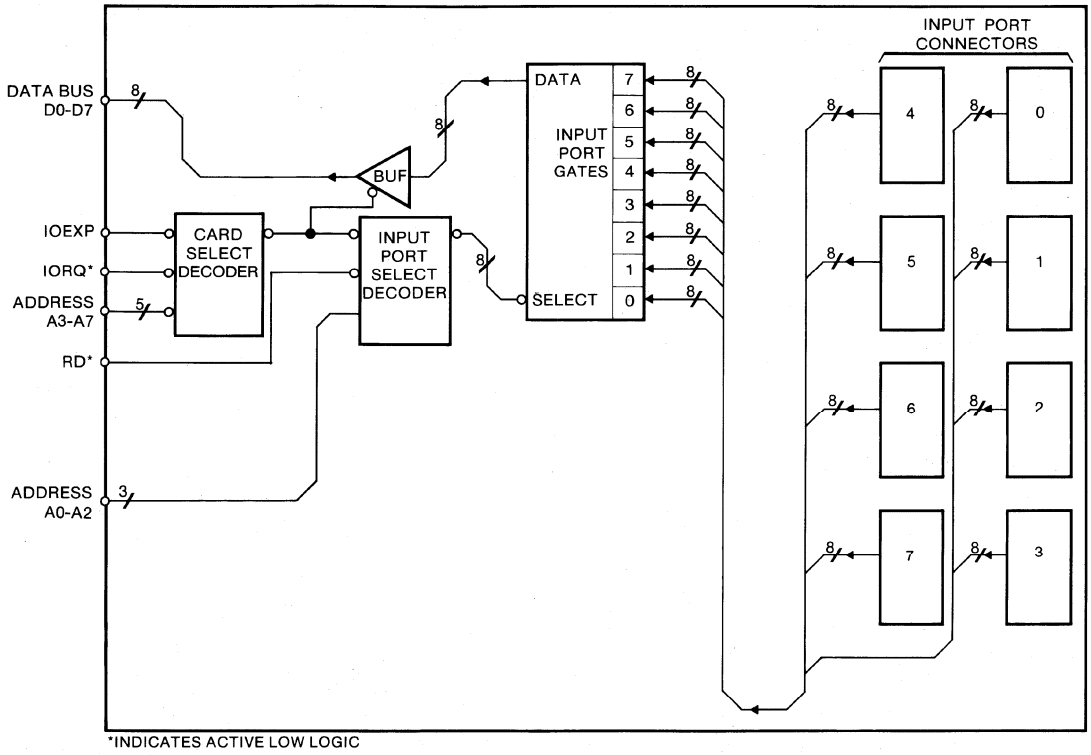


Figure 1-2. Block Diagram (7603A)

INSTALLATION

The 7603A operates as part of an STD BUS card rack system. It must be installed in the card rack with the card ejector toward the top (figure 2-1). A card extender such as the Pro-Log 7901 card can be used to access the 7603A for testing and troubleshooting. Cabling instructions for the 16-pin DIP sockets are given on page 2-4.

> **CAUTION**
>
> To prevent possible damage to your STD BUS system make sure power is **off** before inserting a card into the card rack or removing a card from the card rack.

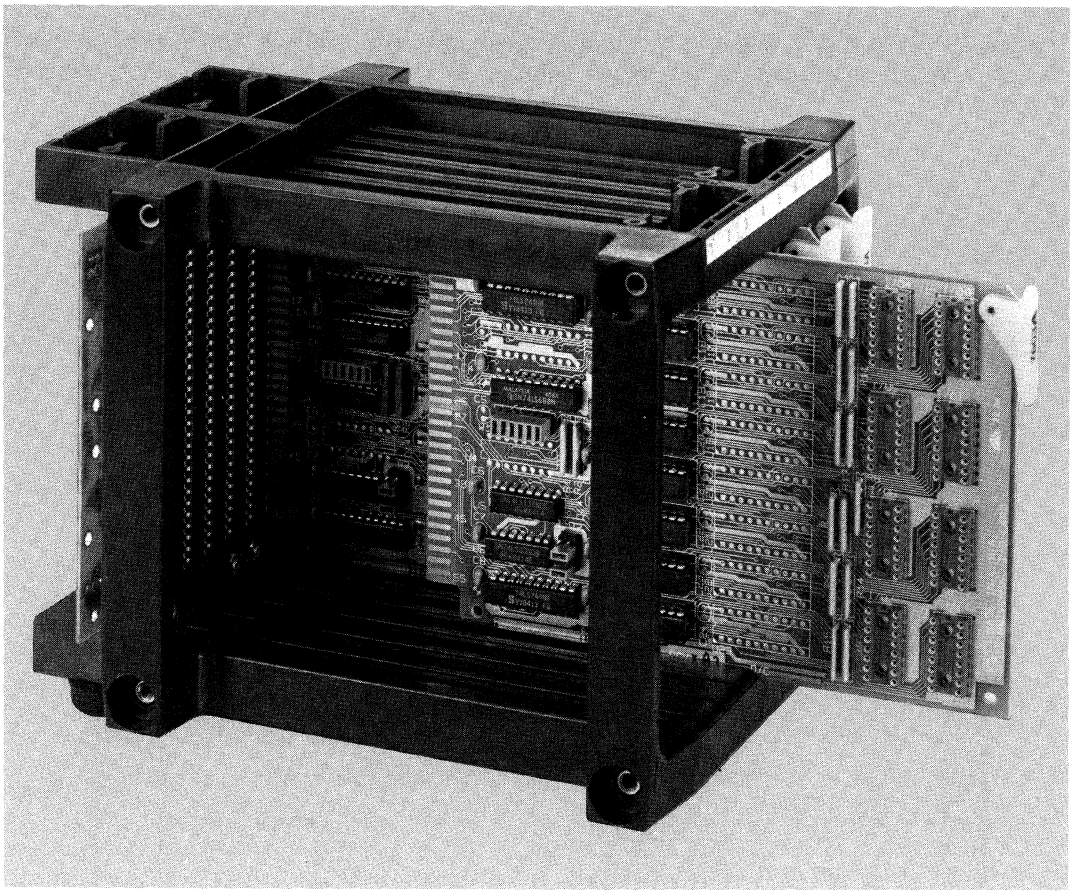


Figure 2-1. Installation (7603A)

I/O MAPPED CARD ADDRESSING

In normal operation the 7603A is addressed directly by the processor card. The 7603A input ports respond to single read instructions executed in the processor operating program. The 7603A is enabled when a jumper-selected combination of address lines A0 through A7 is present and when control lines IORQ*, IOEXP, and RD* are active.

The 7603A occupies eight consecutive I/O port addresses regardless of its mapping assignment. The card is shipped with the eight ports mapped to addresses 00-07. You may retain these addresses or change them by moving the installed jumpers in the W1 header. While the card's port addresses are generally arbitrary, they must differ from all other input port addresses in the system. If they do not differ, multiple cards will respond to the same I/O READ instruction, resulting in BUS contention. The same eight addresses may be used for output ports.

CHANGING THE PORT ADDRESS

The 7603A can be remapped anywhere within the 256-port addressing range of most processors. To change the I/O addressing of the 7603A, move the jumpers in the W1 header. Figure 2-2 shows the W1 header location and jumper installation as shipped. Figure 2-3 shows the jumper positions required for alternate mapping. Note that the jumpers in W2 must remain as shipped for the 7603A to function properly.

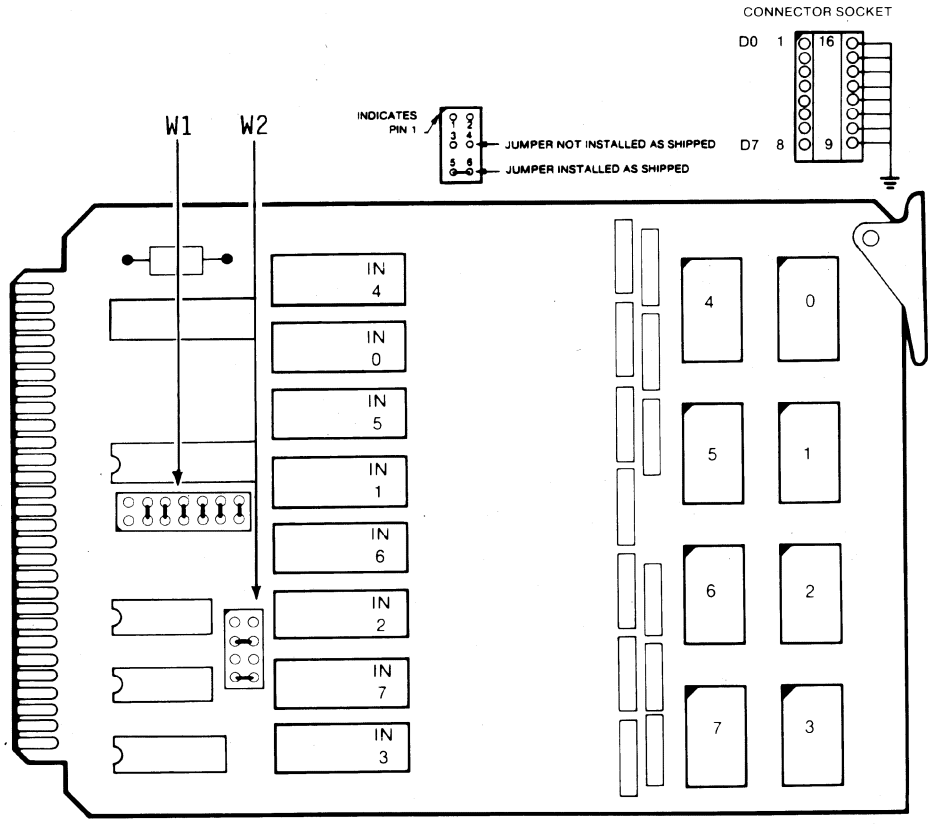


Figure 2-2. Location of Features (7603A)

IOEXP

IOEXP is the I/O expansion line of the STD BUS which allows a system to access 512 I/O ports rather than the standard 256 I/O ports. As shipped, the 7603A is enabled with IOEXP in the low state. Pro-Log processor cards typically connect the IOEXP line to ground. The 7603A can be enabled with IOEXP high by removing jumper W1, 7-8.

ADDRESS RANGE	W1						
	1-2	3-4	5-6	7-8	9-10	11-12	13-14
00 — 07		●	●		●	●	●
08 — 0F			●		●	●	●
10 — 17		●			●	●	●
18 — 1F					●	●	●
20 — 27		●	●		●	●	
28 — 2F			●		●	●	
30 — 37		●			●	●	
38 — 3F					●	●	
40 — 47		●	●		●		●
48 — 4F			●	S	●		●
50 — 57		●		E	●		●
58 — 5F				E	●		●
60 — 67		●	●		●		
68 — 6F			●	N	●		
70 — 77		●		O	●		
78 — 7F				T	●		
80 — 87		●	●	E		●	●
88 — 8F			●			●	●
90 — 97		●		1		●	●
98 — 9F						●	●
A0 — A7		●	●			●	
A8 — AF			●			●	
B0 — B7		●				●	
B8 — BF						●	
C0 — C7		●	●				●
C8 — CF			●				●
D0 — D7		●					●
D8 — DF							●
E0 — E7		●	●				
E8 — EF			●				
F0 — F7		●					
F8 — FF							

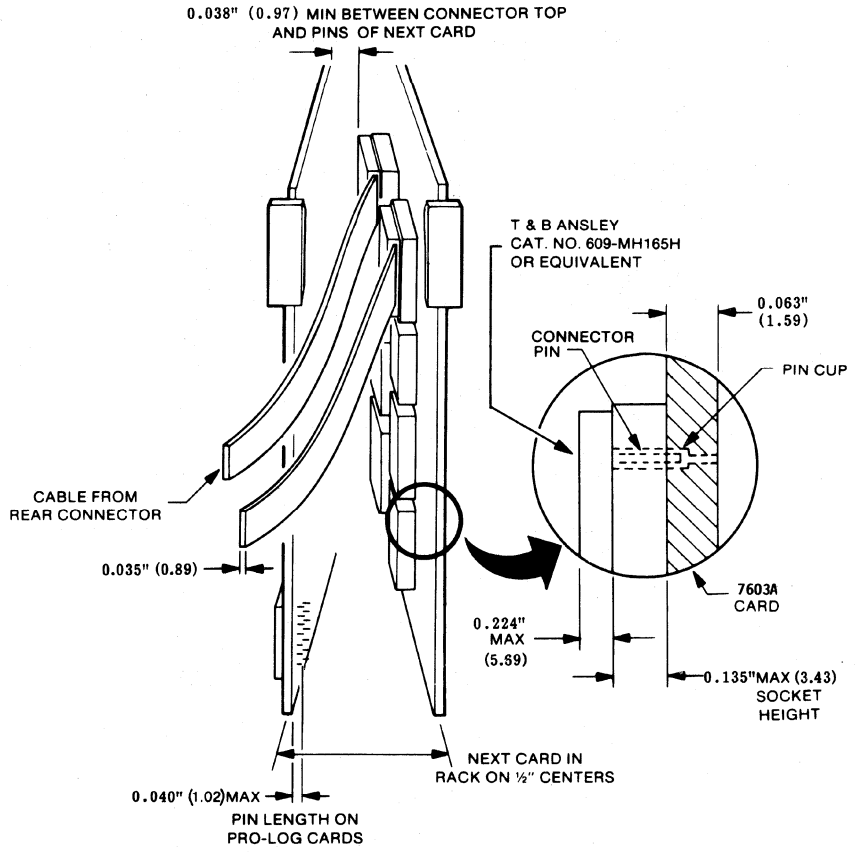
NOTES:
1. For explanation of Jumper W1; 7-8 refer to the "IOEXP" heading.
2. Dot ● indicates jumper installed.
3. Jumpers W2, 3-4 and 7-8 installed.

Figure 2-3. Address Selection Jumpers (7603A)

CABLING

Figure 2-2 (page 2-2) shows the connector associated with each port and the relation of pins to data lines. If the cards are on 1/2-inch centers, use a low-profile connector (figure 2-4). This allows the cable from the rear set of plugs to pass over the outer set. A low-profile connector is suggested, such as T and B Ansley Catalog part number 609-MH165H or equivalent. The connectors should have gold-plated pins to take full advantage of the noncorrosive, high-contact ability provided by the gold-plated contacts in the sockets. The connectors have a high retention rate, preventing the plugs from working loose under normal conditions.

The distance a cable can be extended depends upon the environment. Load characteristics of the buffers are given at the end of this section. Using alternating ground lines helps reduce noise sensitivity.


0.038" (0.97) MIN BETWEEN CONNECTOR TOP AND PINS OF NEXT CARD
T & B ANSLEY CAT. NO. 609-MH165H OR EQUIVALENT
0.063" (1.59)
CONNECTOR PIN
PIN CUP
CABLE FROM REAR CONNECTOR
0.035" (0.89)
7603A CARD
0.224" MAX (5.69)
0.135"MAX (3.43) SOCKET HEIGHT
NEXT CARD IN RACK ON ½" CENTERS
0.040" (1.02)MAX
PIN LENGTH ON PRO-LOG CARDS

Dimensions in millimeters shown in parentheses.

Figure 2-4. Low-Profile Connector (7603A)

SPECIFICATIONS

Mechanical

The 7603A meets all mechanical specifications of the STD BUS. For information on cabling and suggested connectors refer to Cabling, page 2-4.

Electrical and Environmental

	RECOMMENDED OPERATING LIMITS			ABSOLUTE NONOPERATING LIMITS		
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**MAX**	**UNITS**
Free Air Temp	0	+25	+65	-40	+75	°C
Noncondensing Relative Humidity	5	—	95	5	95	%RH
Supply Voltage	4.75	5.00	5.25	0	5.50	V
Supply Current	—	400	644	—	—	mA

Figure 2-5. Electrical and Environmental Specifications (7603A)

STD BUS Interface

See figure 2-6 for the 7603A-to-STD BUS interface specifications.

Port Interface

Voltage Level:	TTL
Input Load:	4 LSTTL loads
Input Hysteresis:	0.2V minimum 0.4V typical

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
+5V	IN		2	1		IN	+5V
GROUND	IN		4	3		IN	GROUND
-5V			6	5			-5V
D7		55	8	7	55		D3
D6		55	10	9	55		D2
D5		55	12	11	55		D1
D4		55	14	13	55		D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		3	A2
A9			28	27		1	A1
A8			30	29		1	A0
RD*	1		32	31		3	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX			36	35		1	IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

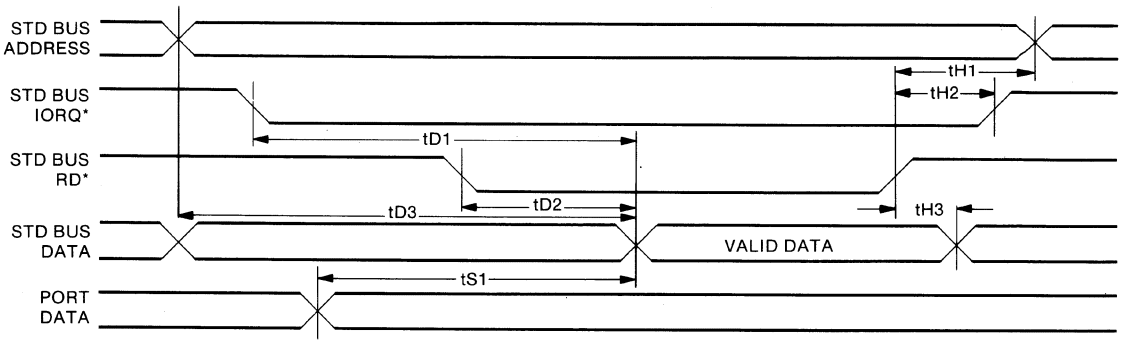
* Designates active low-level logic

Figure 2-6. 7603A/STD BUS Interface Specifications

Timing

Timing data is specified at the following conditions:

V_{CC}:	4.75 to 5.25V
T:	0 to 65°C
Capacitive Load:	45 pf on STD BUS



SYMBOL	PARAMETER	NANOSECONDS MIN	NANOSECONDS MAX
tD1	Data delay from IORQ* active		150
tD2	Data delay from RD* active		125
tD3	Data delay from address valid		130
tH1	Address hold after RD* inactive	40	
tH2	IORQ* hold after RD* inactive	45	
tH3	Data hold after RD* inactive	90	
tS1	Port data setup before STD data valid	45	

Figure 2-7. Read Timing (7603A)

OPERATION

To operate the 7603A input card, simply read from the desired port. The data is not inverted.

Section 4

OPERATING SOFTWARE

Section 4 is normally reserved for software. The 7603A requires no special software.

REFERENCE DRAWINGS

The schematic (figure 5-1) and assembly drawing (figure 5-2) in the following pages are included in this manual FOR REFERENCE USE ONLY. These drawings may differ in some respects from the card you receive from Pro-Log. If you require the specific revision documents of the schematic and assembly for the board shipped, please use the information request form in the back of this manual to order them.

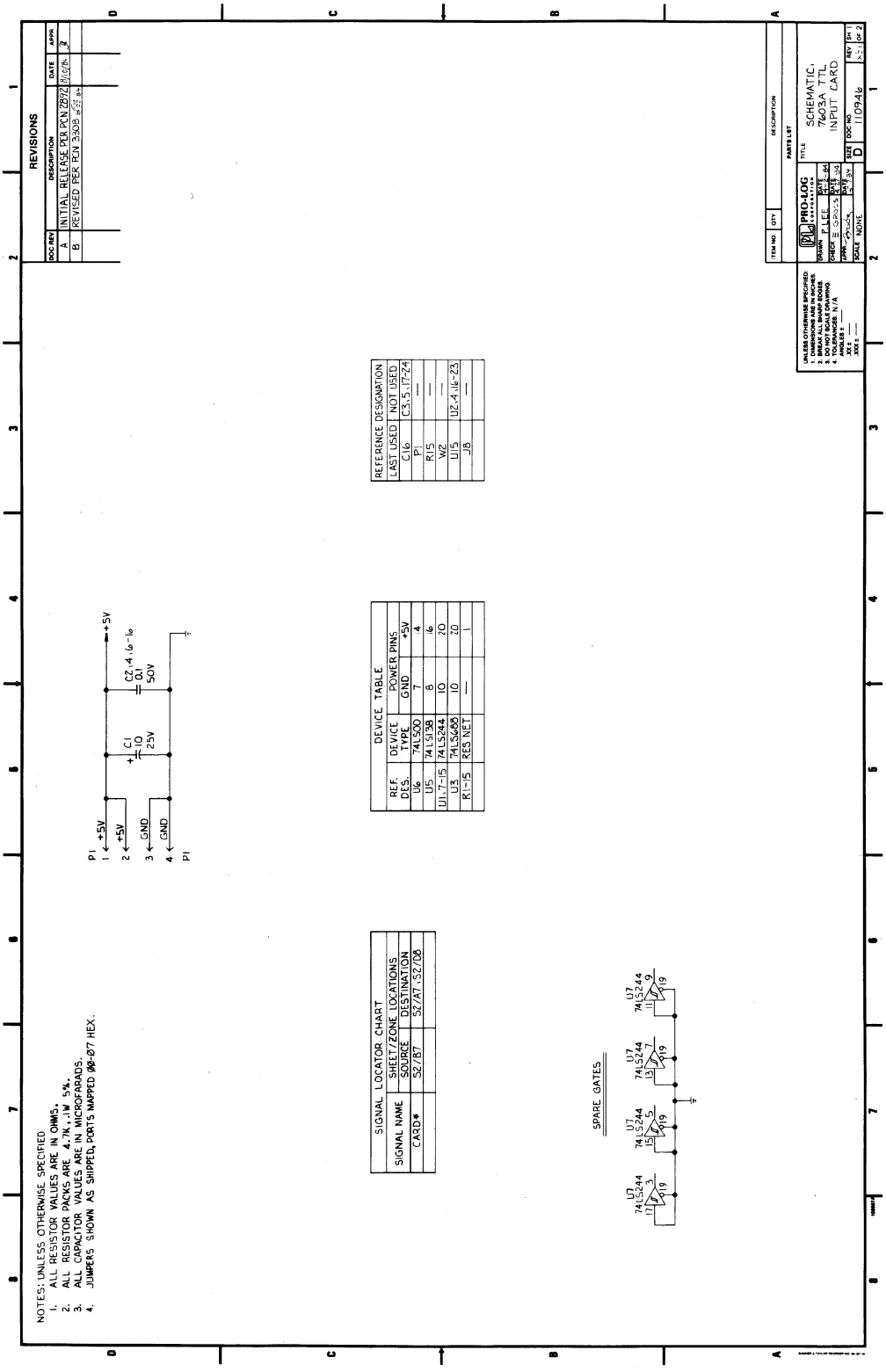


Figure 5-1. Schematic (7603A)
(FOR REFERENCE ONLY)

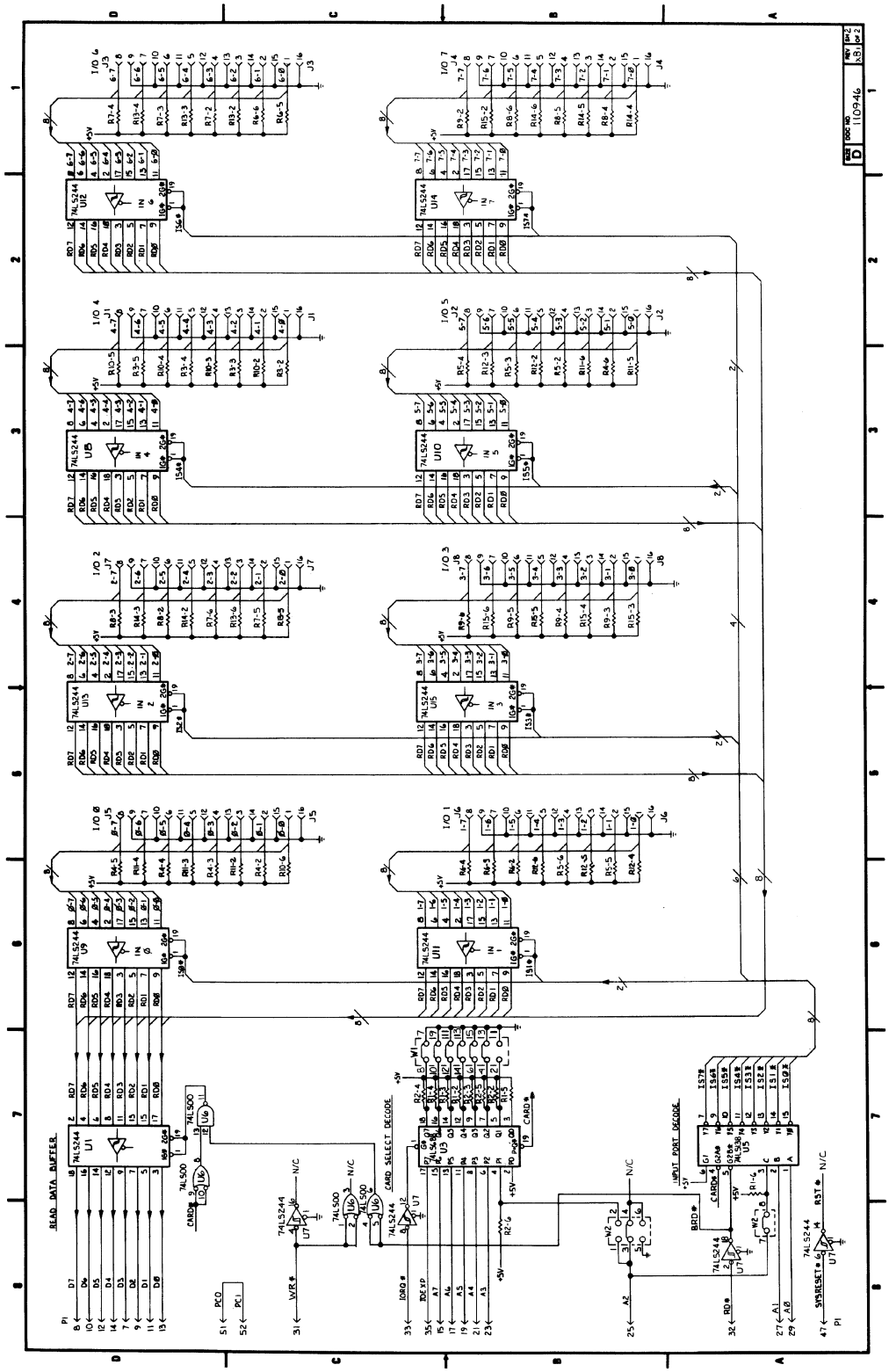


Figure 5–1. Schematic (7603A) Continued
(FOR REFERENCE ONLY)

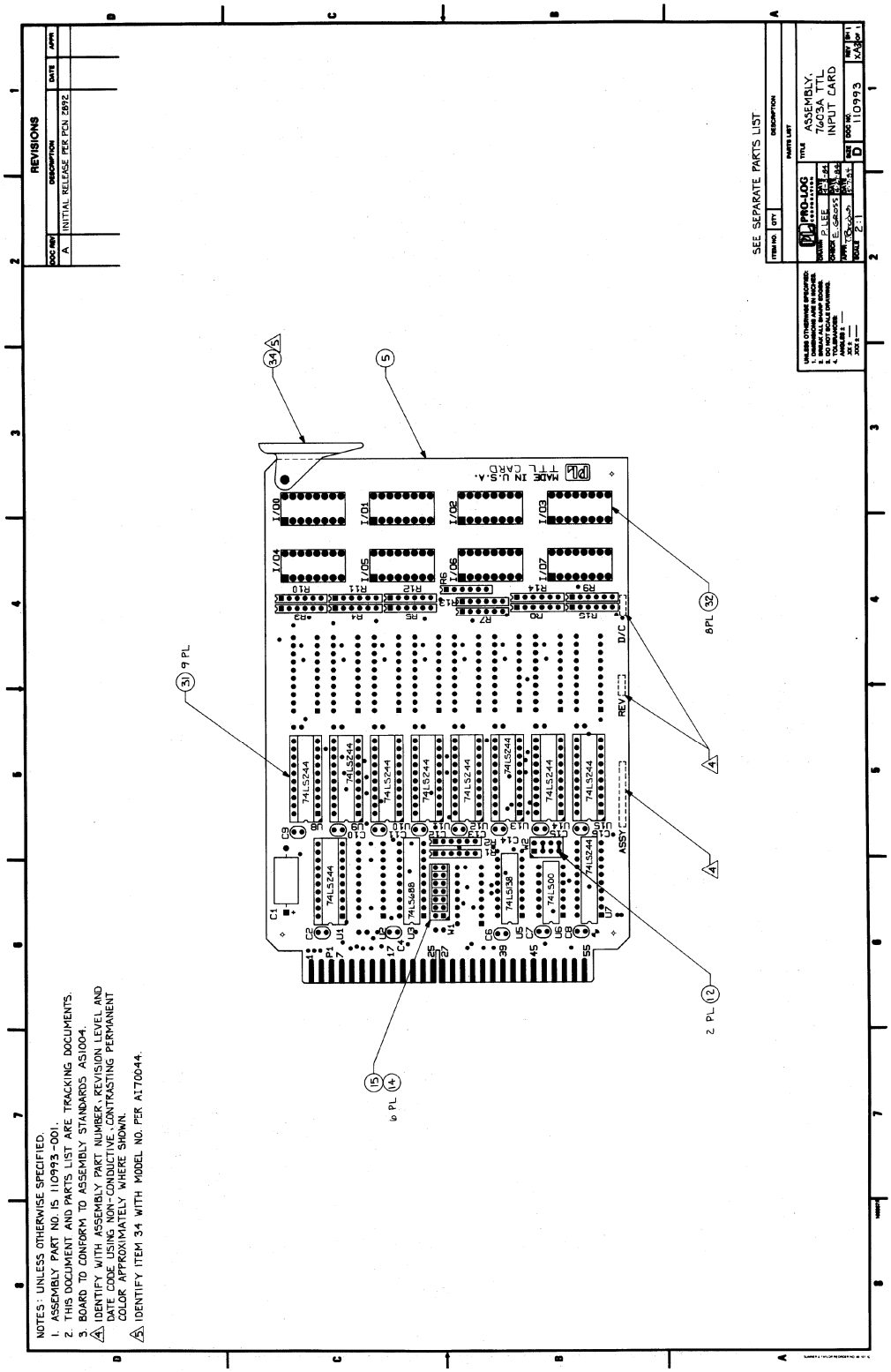

REVISIONS
DESCRIPTION
INITIAL RELEASE PER PCN 2892
SEE SEPARATE PARTS LIST
PRO-LOG
ASSEMBLY, 7603A TTL INPUT CARD
110993
NOTES: UNLESS OTHERWISE SPECIFIED.
1. ASSEMBLY PART NO. IS 110993-001.
2. THIS DOCUMENT AND PARTS LIST ARE TRACKING DOCUMENTS.
3. BOARD TO CONFORM TO ASSEMBLY STANDARDS AS1004.
4. IDENTIFY WITH ASSEMBLY PART NUMBER, REVISION LEVEL AND DATE CODE USING NON-CONDUCTIVE, CONTRASTING PERMANENT COLOR APPROXIMATELY WHERE SHOWN.
5. IDENTIFY ITEM 34 WITH MODEL NO. PER A170044.
MADE IN U.S.A.
8 PL
9 PL
2 PL
6 PL
D/C
REV
ASSY

Figure 5-2. Assembly (7603A)
(FOR REFERENCE ONLY)

STD 7000

7604A

TTL INPUT/OUTPUT CARD

USER'S MANUAL

CONTENTS

	Page
Figures	iii
Section 1 - Purpose and Main Features	1-1
Purpose	1-1
Features	1-1
Section 2 - Installation and Specifications	2-1
Installation	2-1
Selecting a Configuration	2-2
I/O Mapped Card Addressing	2-5
Changing the Port Address	2-5
IOEXP	2-7
Address Mapping	2-7
Cabling	2-9
Specifications	2-10
Timing	2-12
Section 3 - Operation and Programming	3-1
Operation	3-1
Section 4 - Operating Software	4-1
Section 5 - Maintenance	5-1
Reference Drawings	5-1

FIGURES

Figure		Page
1-1	7604A	1-1
1-2	Block Diagram	1-2
2-1	Installation	2-1
2-2	Available Functions	2-2
2-3	Configuring for a Function	2-3
2-4	Port Options for a 7604A Configuration	2-4
2-5	Location of Features	2-6
2-6	Address Selection Jumpers	2-8
2-7	Low-Profile Connector	2-9
2-8	Electrical and Environmental Specifications	2-10
2-9	7604A/STD BUS Interface Specification	2-11
2-10	Read Timing	2-12
2-11	Write Timing	2-12
5-1	Schematic	5-2
5-2	Assembly	5-4

PURPOSE

The 7604A provides eight 8-bit TTL I/O ports, 64 I/O lines total. It will perform all the functions of three other TTL I/O cards by Pro-Log, the 7601A, 7602A, and the 7603A. Each of the eight ports on the 7604A can be independently configured to one of the following:

- Input port
- Output port
- Output port with readback

The I/O lines are noninverting and the outputs can drive 16 LSTTL loads (4 TTL loads). The card decodes eight address lines and the STD BUS IOEXP signal. Slip-on connectors allow mapping to any consecutive group of I/O addresses. The STD BUS SYSRESET* signal clears all output ports simultaneously.

FEATURES

- Eight 8-bit I/O ports, 64 lines
- Each port can be configured as an input, output, or output with readback
- Outputs drive 16 LSTTL loads (4 TTL loads)
- Inputs present 4 LSTTL (1 TTL) loads
- Can occupy four or eight consecutive I/O addresses
- Flexible I/O mapping
- +5V operation
- Universal processor compatibility

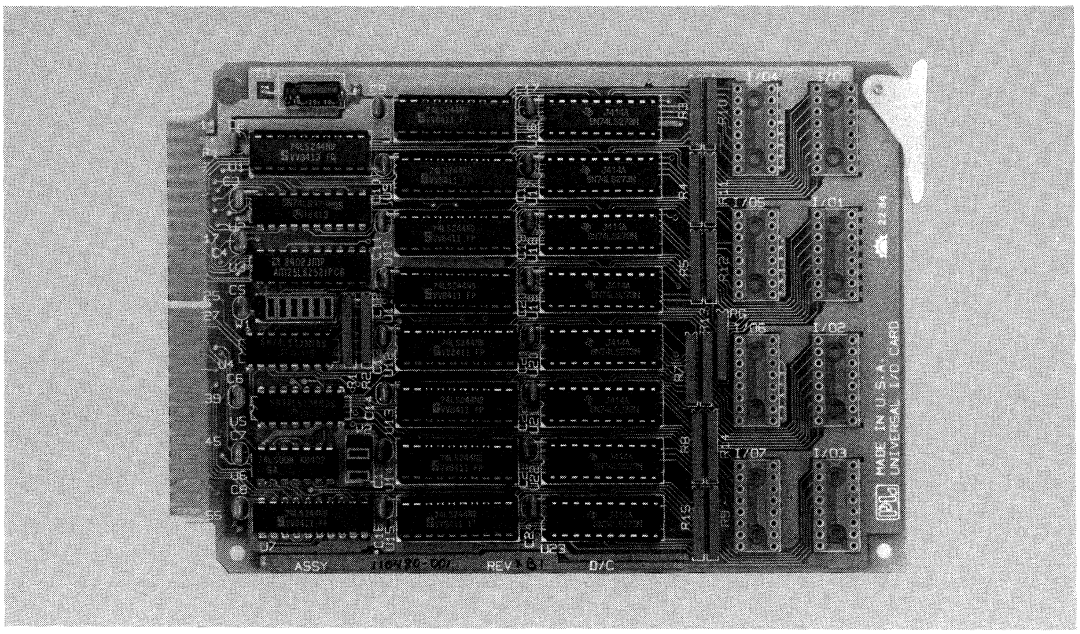


Figure 1-1. 7604A

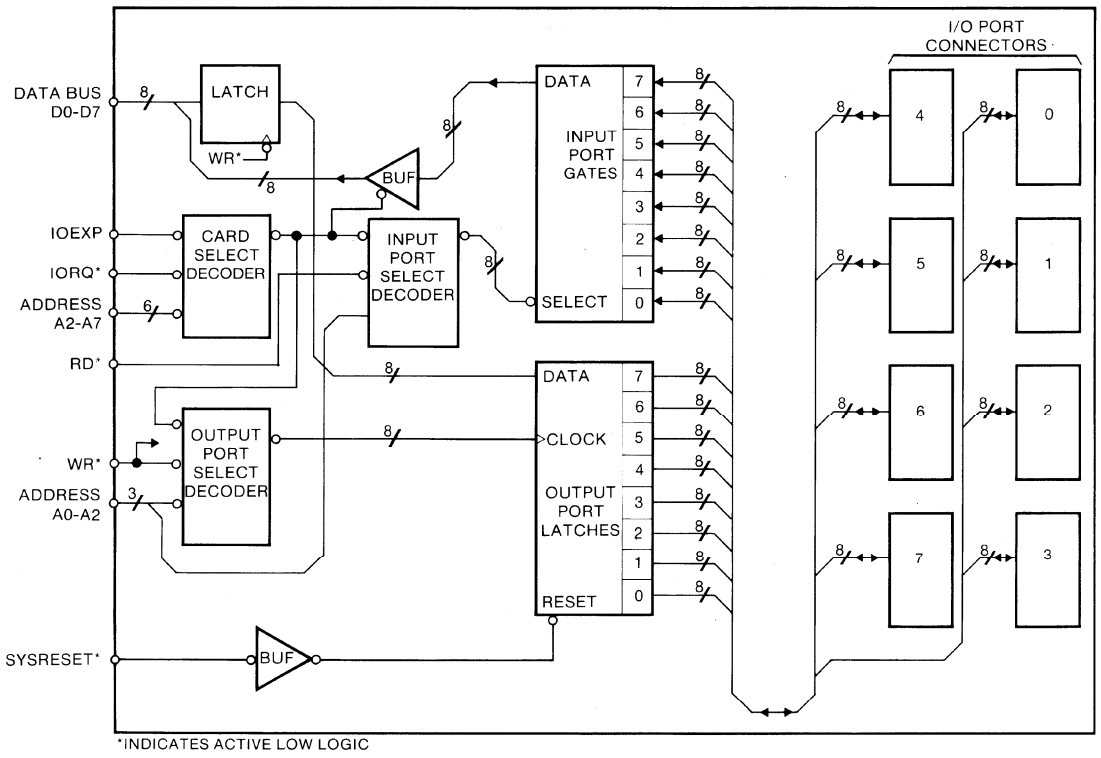


Figure 1-2. Block Diagram (7604A)

INSTALLATION

The 7604A operates as part of an STD BUS card rack system. It must be installed in the card rack with the card ejector toward the top (figure 2-1). A card extender such as the Pro-Log 7901 card can be used to gain access to the 7604A for testing and troubleshooting. Cabling instructions for the 16-pin DIP sockets are given on page 2-4.

CAUTION

To prevent possible damage to your STD BUS system make sure power is **OFF** before inserting a card into the card rack or removing a card from the card rack.

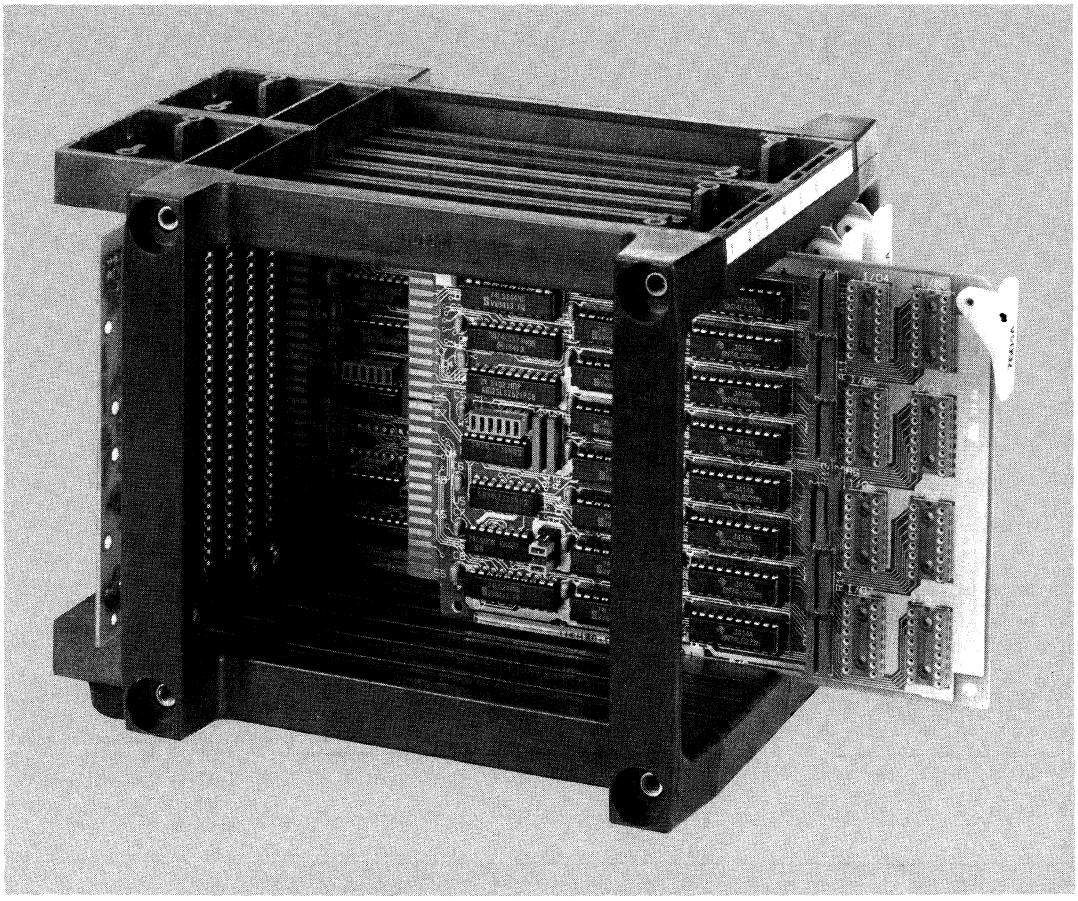


Figure 2-1. Installation (7604)

SELECTING A CONFIGURATION

The 7604A has eight ports that can be individually configured as input, output, or as output with readback. These configurations make it possible for the 7604A to perform all functions possible with the Pro-Log 7601A, 7602A, and 7603A. These configurations are summarized in figure 2-2.

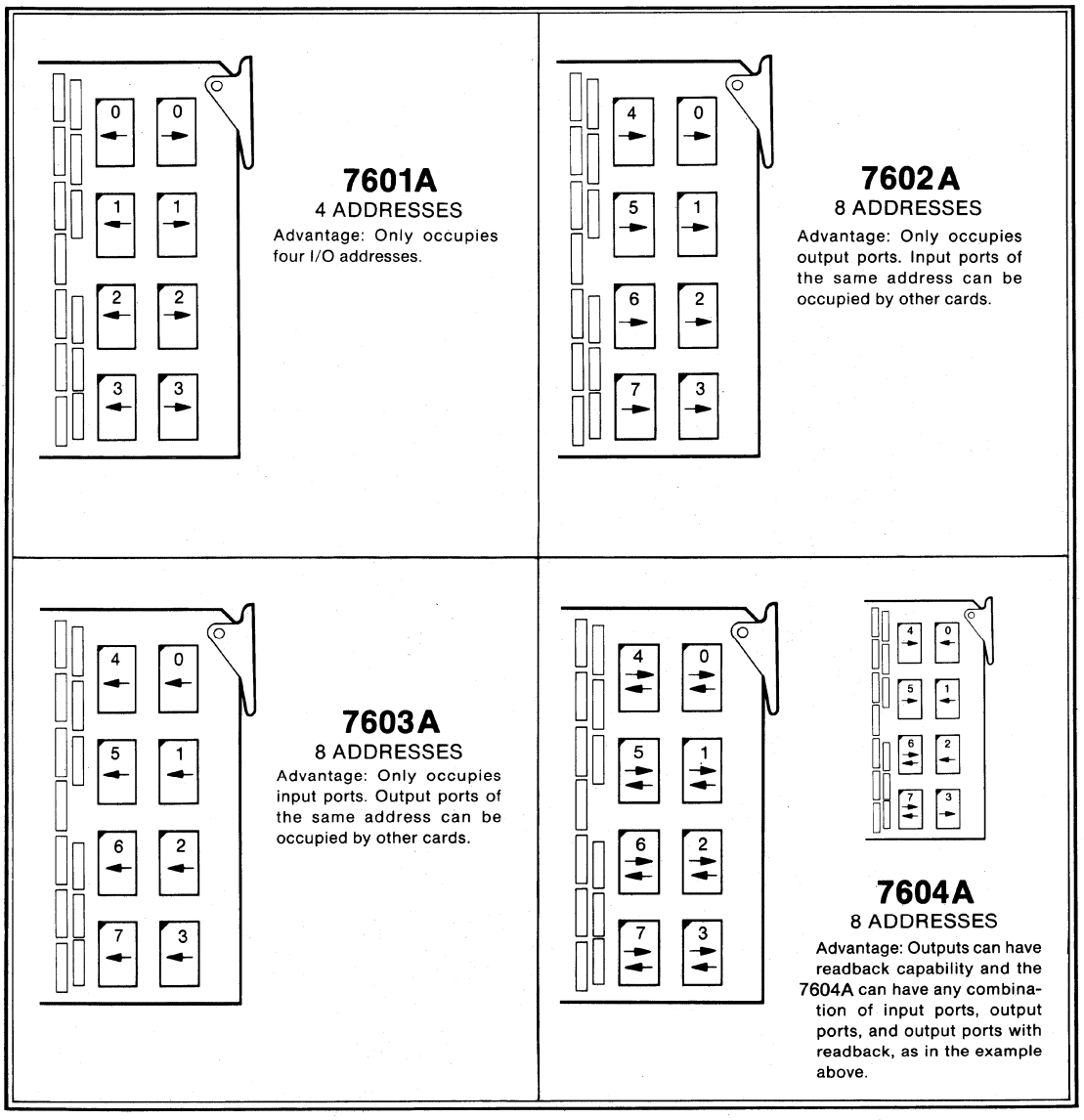

7601A
4 ADDRESSES
Advantage: Only occupies four I/O addresses.
7602A
8 ADDRESSES
Advantage: Only occupies output ports. Input ports of the same address can be occupied by other cards.
7603A
8 ADDRESSES
Advantage: Only occupies input ports. Output ports of the same address can be occupied by other cards.
7604A
8 ADDRESSES
Advantage: Outputs can have readback capability and the 7604A can have any combination of input ports, output ports, and output ports with readback, as in the example above.

Figure 2-2. Available Functions (7604A)

Refer to figure 2-3 to adapt the 7604A for your selected function. ICs may need to be removed and wire jumpers may need to be changed. Input buffers on output ports may be left installed for readback.

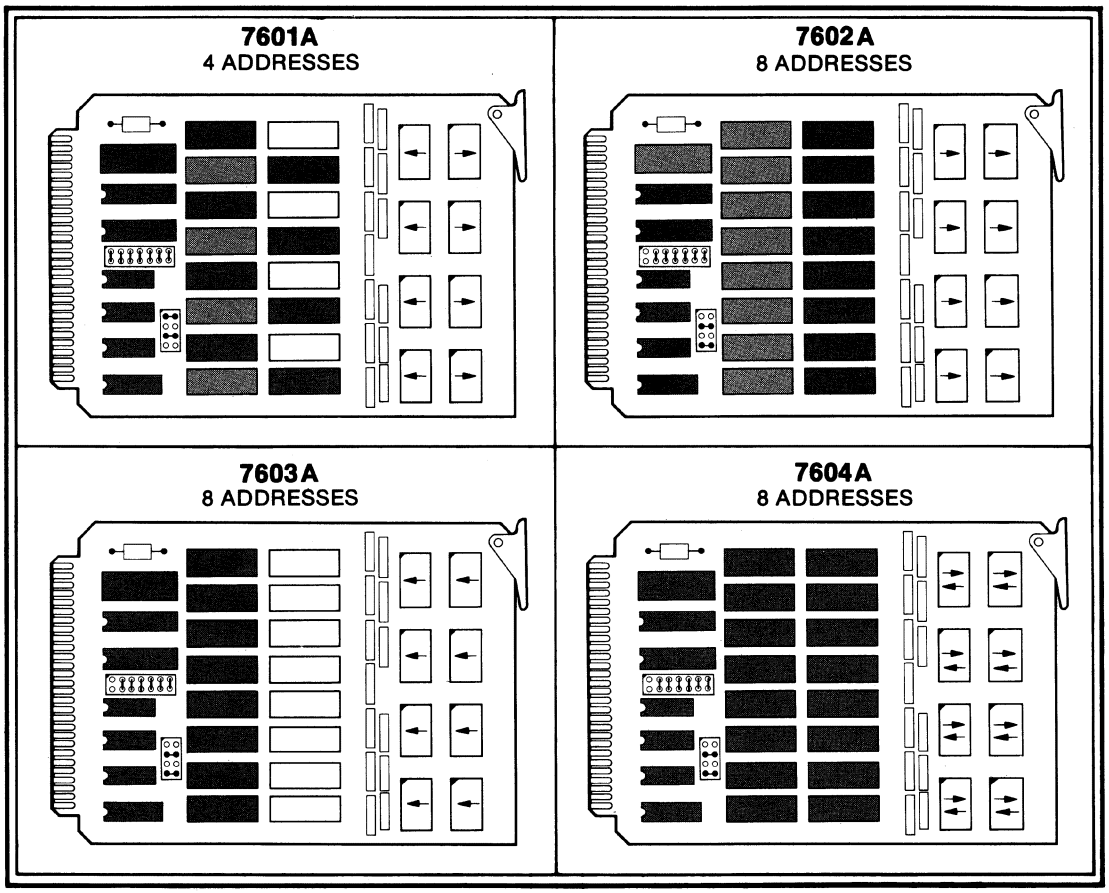
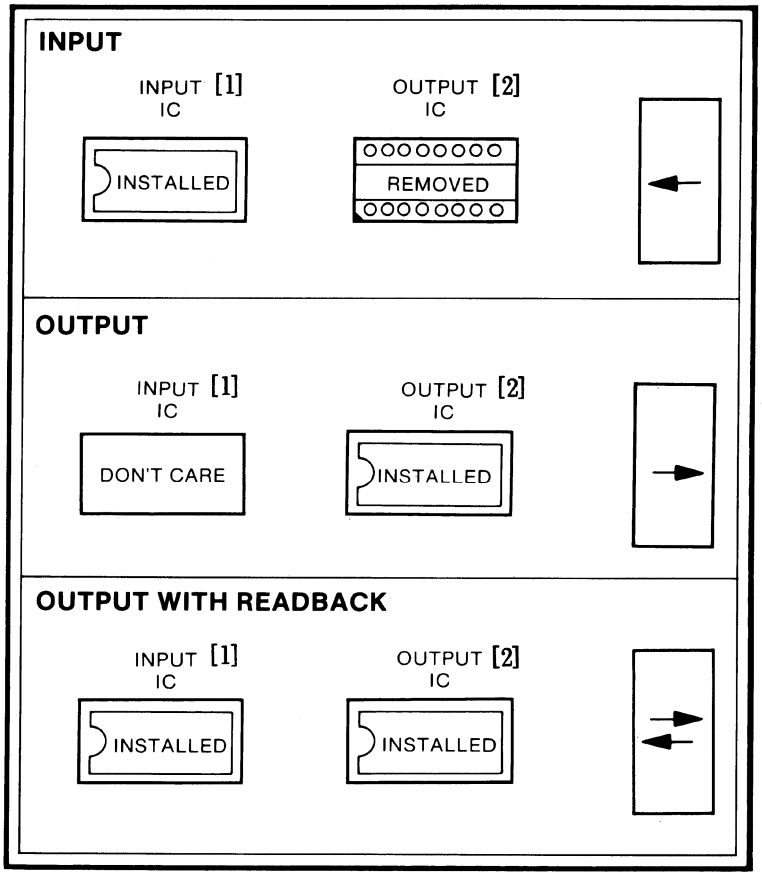


Figure 2-3. Configuring for a Function

The 7604A configuration can have the standard eight output ports with readback capability or a combination of inputs, outputs, and outputs with readback. Figure 2-4 shows how to select the desired function for a given port. Figure 2-5 shows which connector is associated with each port and which ICs perform the input and output functions for each port.

For an input function, the output latch IC must be removed. For an output function, the input buffer IC does not need to be removed. The input ability can be ignored. In any case, each of the eight ports on a 7604A configuration still occupy both the input and output port functions of that address. If an IC has been removed, that function is simply inoperable.



[1] INPUT IC = 74LS244
[2] OUTPUT IC = 74LS273

Figure 2-4. Port Options for a 7604A Configuration

I/O MAPPED CARD ADDRESSING

In normal operation, the 7604A is addressed directly by the processor card. The 7604A input and output ports respond to single read and write instructions executed in the processor operating program. The 7604A is enabled when a jumper-selected combination of address lines A0 through A7 is present, and when the following control lines are active: IORQ*, IOEXP, and either RD* or WR*.

The 7604A occupies four or eight consecutive I/O addresses depending upon its mapping assignment. The card is shipped with the eight ports mapped to addresses 00-07. You may retain these addresses or change them by moving the installed slip-on connectors in W1 header. While the card's port addresses are generally arbitrary, they must differ from all other I/O port addresses in the system. If they do not differ, multiple cards will respond to the same I/O READ instruction, resulting in bus contention.

CHANGING THE PORT ADDRESS

The 7604A can be remapped anywhere within the 256-port addressing range of most processors. To change the I/O addressing of the 7604A, move slip-on connectors in the W1 header. Figure 2-5 shows where the W1 header is located and where the slip-on connectors are installed when shipped. Figure 2-6, page 2-8, shows the jumper positions required for alternate mapping.

JUMPER GROUP		DESCRIPTION
W1	1-2	Used for mapping the 4 I/O Address configurations (see figures 2-2 and 2-6)
	3-4	Used for mapping (see figure 2-6)
	5-6	Used for mapping (see figure 2-6)
	9-10	Used for mapping (see figure 2-6)
	11-12	Used for mapping (see figure 2-6)
	13-14	Used for mapping (see figure 2-6)
	7-8	Installed — Card enabled with IOEXP low Removed -- Card enabled with IOEXP high
W2	1-2	4 I/O Address configurations
	5-6	4 I/O Address configurations
	3-4	8 I/O Address configurations
	7-8	8 I/O Address configurations

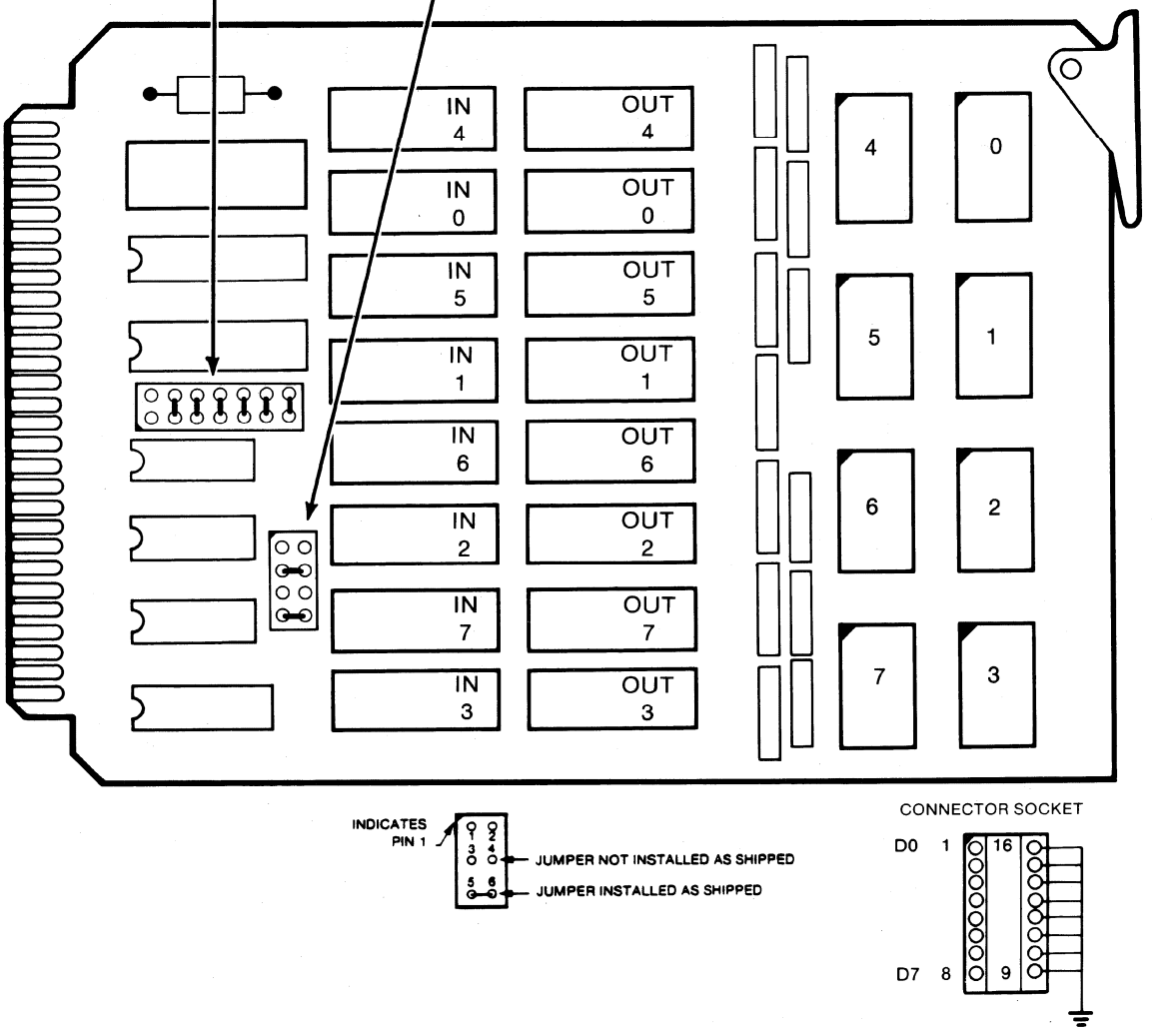


Figure 2-5. Location of Features (7604A)

IOEXP

IOEXP is the I/O expansion line of the STD BUS which allows a system to access 512 I/O ports rather than the standard 256 I/O ports. As shipped, the 7604A is enabled with IOEXP in the low state. Pro-Log processor cards typically connect the IOEXP line to ground. The 7604A can be enabled with IOEXP high by removing jumper W1, 7-8.

ADDRESS MAPPING

Figure 2-6 shows the combination of jumpers in group W1 needed to select a particular address range. The starting address of each address range is shown. One chart is for 7601A configurations in which the card occupies only four I/O addresses. The other chart is for configurations using eight I/O addresses. Be sure the jumpers in group W2 are situated as noted in the figure. Jumper 7-8 is explained under the IOEXP heading.

give the specifications for the 7604A card.

s

chanical specifications of the STD BUS. For information
connectors, refer to Cabling, page 2-8.

ntal

	RECOMMENDED OPERATING LIMITS			ABSOLUTE NONOPERATING LIMITS		
	MIN	TYP	MAX	MIN	MAX	UNITS
	0	+25	+65	-40	+75	°C
ve	5	—	95	5	95	%RH
	4.75	5.00	5.25	0	5.50	V
	—	560[2]	900[1]	—	—	mA

ach 74 LS244 input buffer removed (U1 and U8-U15); subtract 27 mA
ut latch removed (U16-U23).

ach 74LS244 input buffer removed (U1 and U8-U15); subtract 17 mA
ut latch removed (U16-U23).

8. Electrical and Environmental Specifications (7604A)

loads
ds
inimum; 0.4V typical

SPECIFICA

Mechanical

The 7601A
on cabling

Electrical

PARAMET
Free Air Temp
Noncondensing Humidity
Supply Voltage
Supply Curren

STD BUS I

See figure

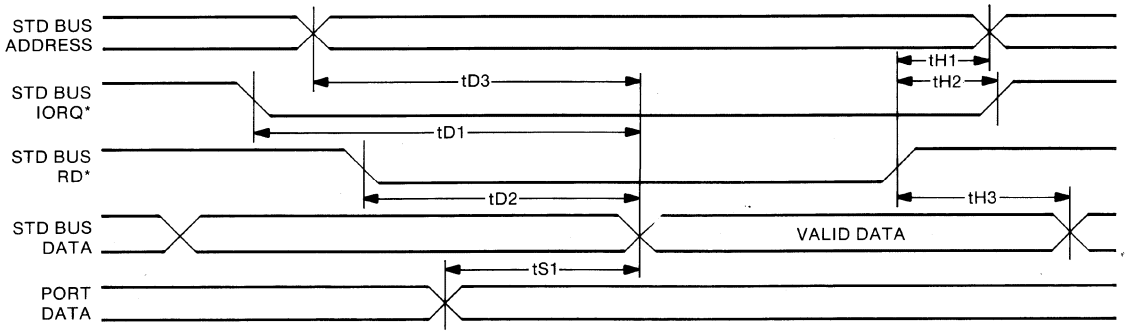
Port Interf

Voltage Le
Output Dri
Input Load
Input Hyst

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
+5V	IN		2	1		IN	+5V
GROUND	IN		4	3		IN	GROUND
-5V			6	5			-5V
D7	1	55	8	7	55	1	D3
D6	1	55	10	9	55	1	D2
D5	1	55	12	11	55	1	D1
D4	1	55	14	13	55	1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		4	A2
A9			28	27		2	A1
A8			30	29		2	A0
RD*	1		32	31		3	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX			36	35		1	IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

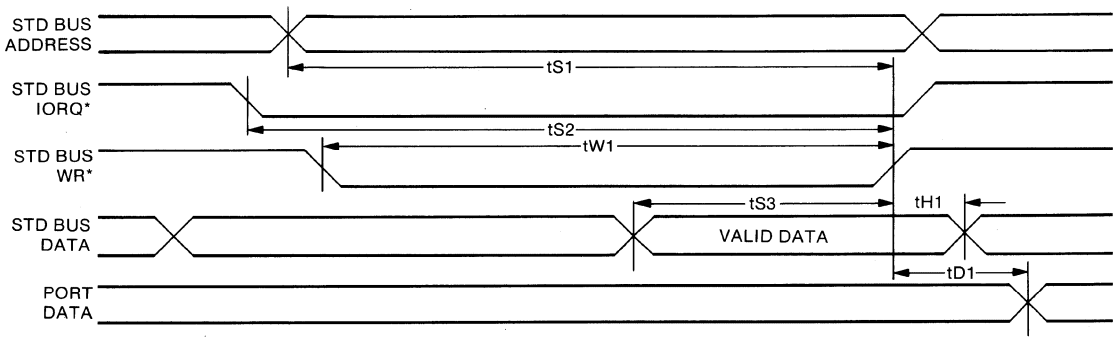
* Designates active low-level logic

Figure 2-9. 7604A/STD BUS Interface Specification



SYMBOL	PARAMETER	NANOSECONDS MIN	NANOSECONDS MAX
tD1	Data delay from IORQ* active		150
tD2	Data delay from RD* active		125
tD3	Data delay from address valid		130
tH1	Address hold after RD* inactive	40	
tH2	IORQ* hold after RD* inactive	45	
tH3	Data hold after RD* inactive	90	
tS1	Port data setup before STD data valid	45	

Figure 2-10. Read Timing (7604A)



SYMBOL	PARAMETER	NANOSECONDS MIN	NANOSECONDS MAX
tD1	Port data delay from WR* inactive		85
tH1	Data hold after WR* inactive	45	
tS1	Address setup before WR* inactive	85	
tS2	IORQ* setup before WR* inactive	100	
tS3	Data setup before WR* inactive	40	
tW1	WR* pulse width	75	

Figure 2-11. Write Timing (7604A)

OPERATION

The operation of the 7604A is to simply write to or read from the desired port. The data is not inverted. Output ports with readback allow the reading or verifying of the current output state. The output latches are two-state, and outputs with readback cannot be used as inputs.

Section 4

OPERATING SOFTWARE

Section 4 is normally reserved for software. The 7604A requires no special software.

REFERENCE DRAWINGS

The schematic (figure 5-1) and assembly drawing (figure 5-2) in the following pages are included in this manual FOR REFERENCE USE ONLY. These drawings may differ in some respects from the card you receive from Pro-Log. If you require the specific revision documents of the schematic and assembly for the board shipped, please use the information request form in the back of this manual to order them.

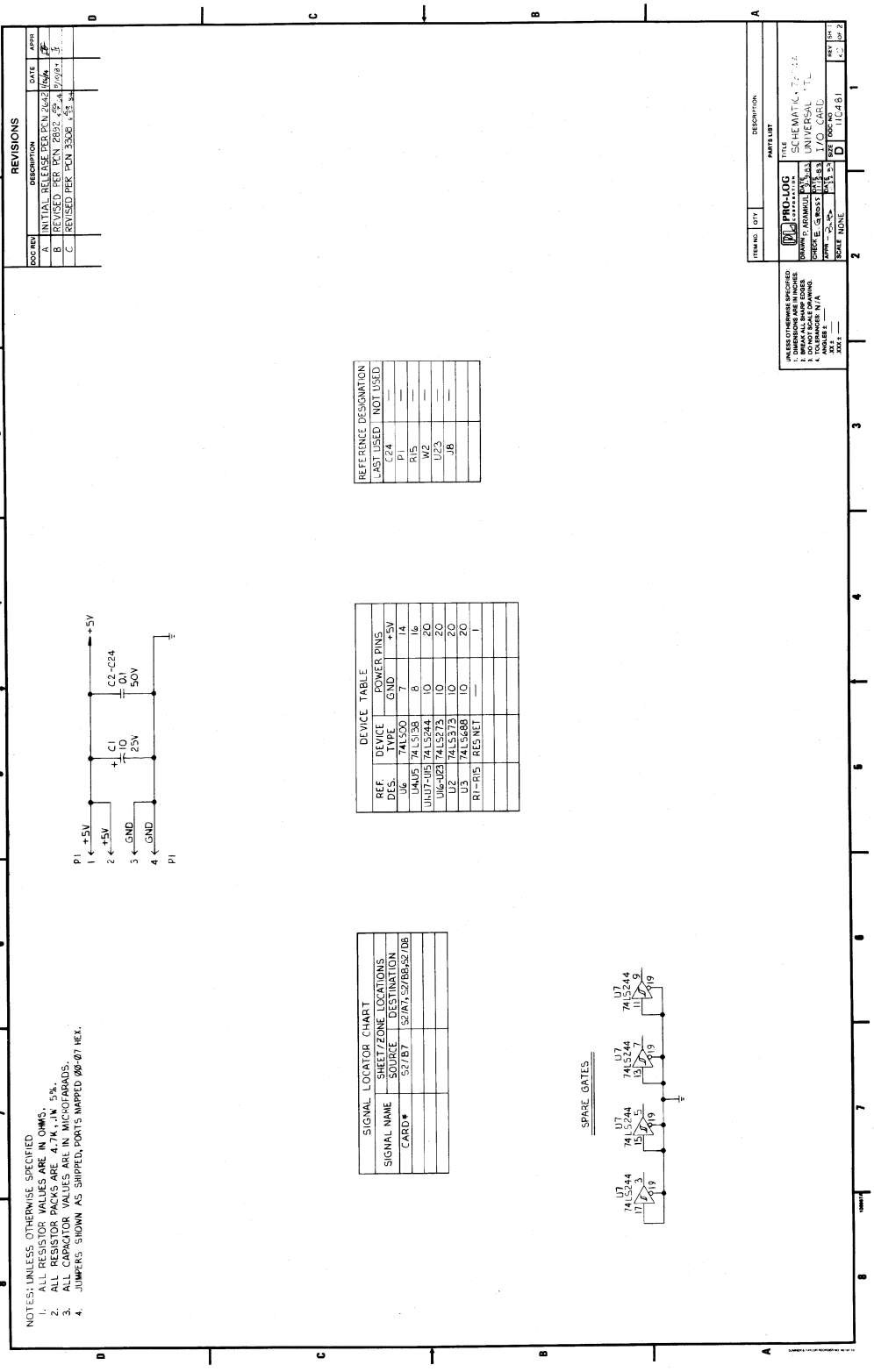


Figure 5-1. Schematic (7604A)
(FOR REFERENCE ONLY)

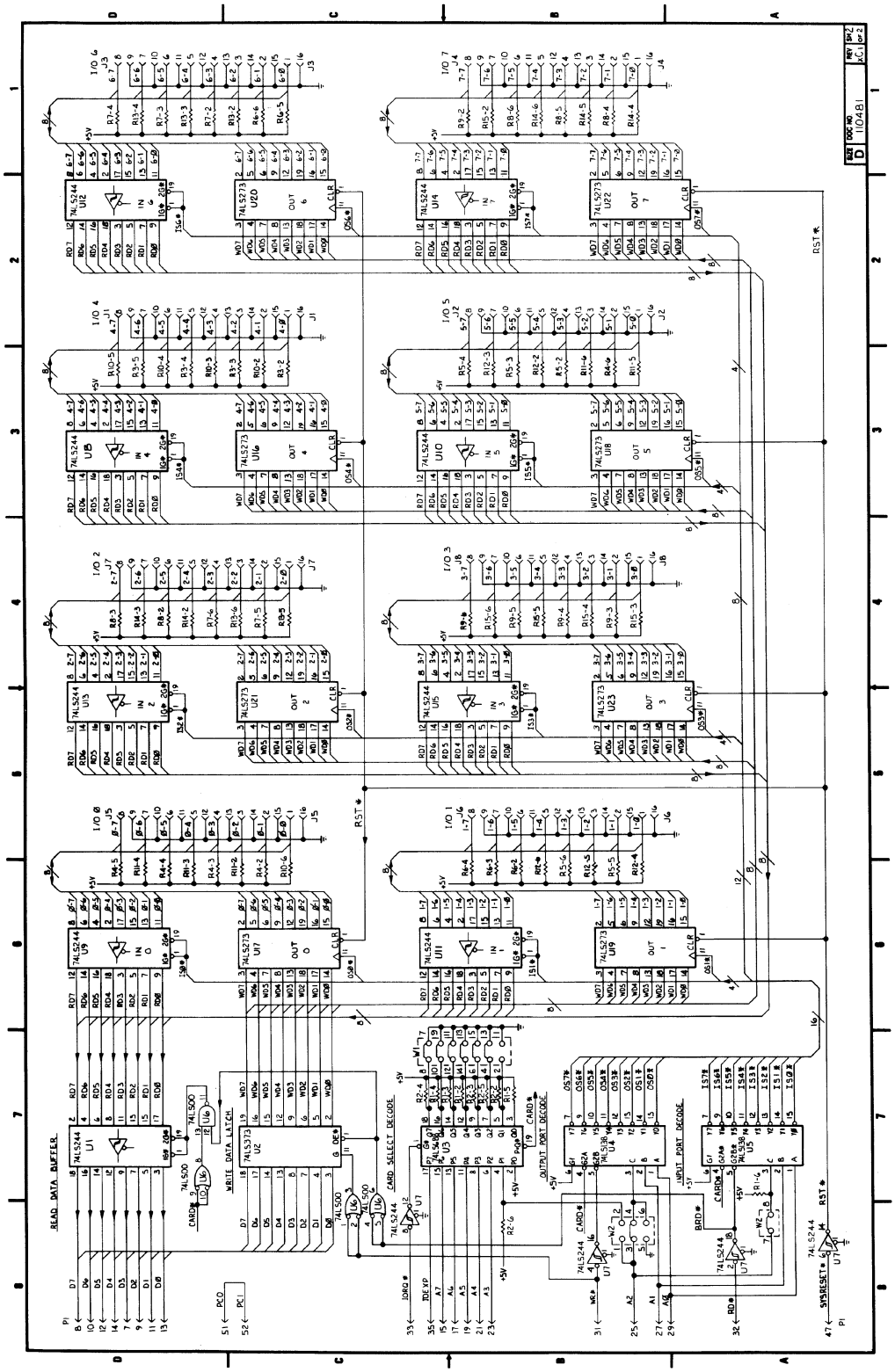


Figure 5-1. Continued
(FOR REFERENCE ONLY)

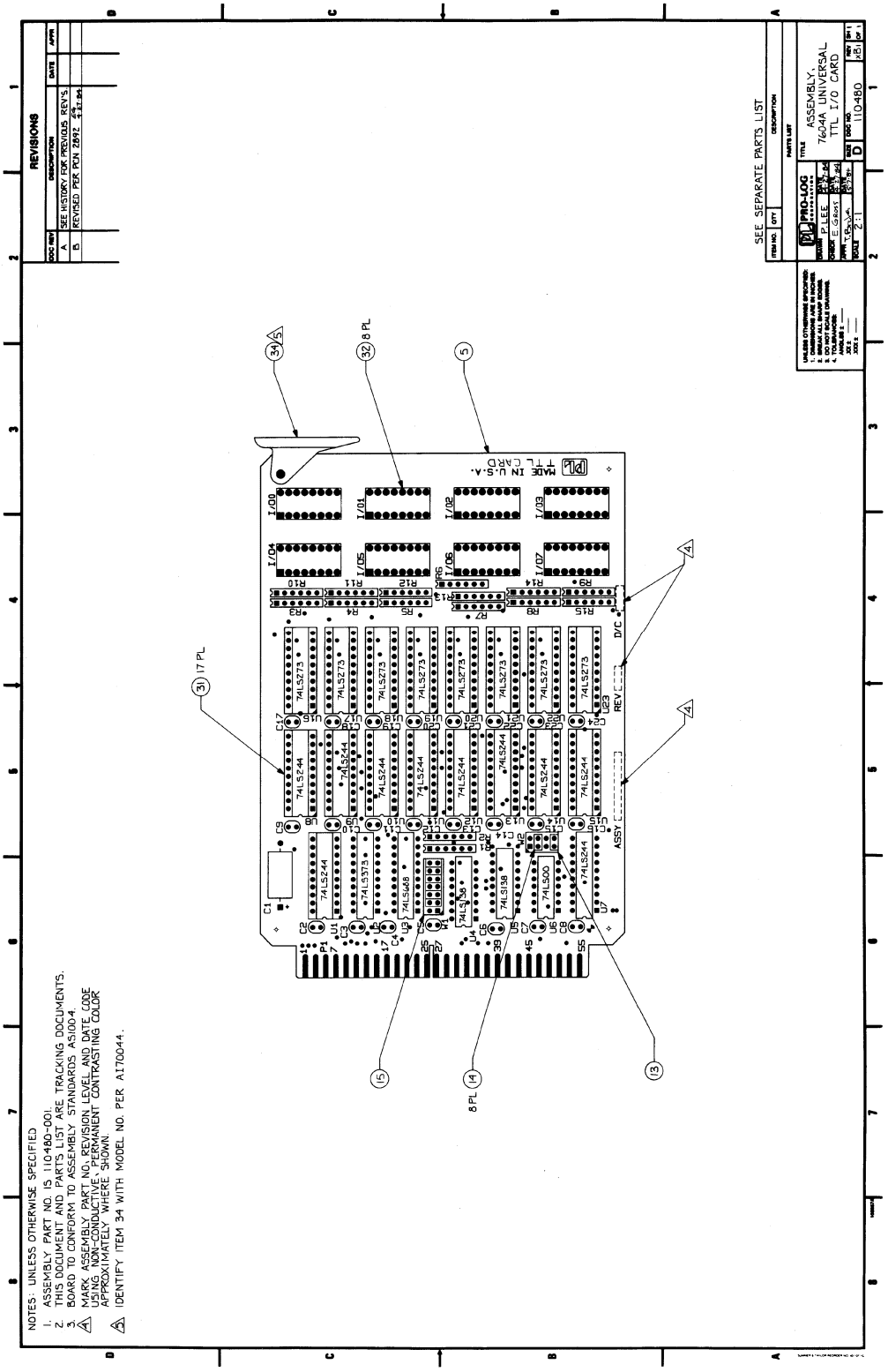


Figure 5-2. Assembly Drawing (7604A)
(FOR REFERENCE ONLY)

RETURN FOR REPAIR PROCEDURES

Domestic Customers:

1. Call CUSTOMER SERVICE at (408) 372-4593 (in California) or (800) 538-9570 (outside of California) 7 AM to 3 PM PST.

2. Explain the problem and we may be able to solve it on the phone. If not, we will give you a Customer Return Order (CRO) number.

   Mark the CRO number on the shipping label, packing slip, and other paperwork accompanying the return. We cannot accept returns without a CRO.

3. Please be sure to enclose a packing slip with the CRO number, the equipment serial number if applicable, and the reason for return. Also enclose the name and telephone number of the person we should contact (preferably the user).

4. Package the equipment in a solid cardboard box secured with packing material.

   CAUTION: Loose MOS integrated circuits, or any product containing CMOS integrated circuits, must be protected from electrostatic discharge during handling. Use conductive foam pads or conductive plastic bags, and never place MOS or CMOS circuitry in contact with Styrofoam materials.

5. Ship prepaid and insured to:

   Pro-Log Corporation
   2411 Garden Road
   Monterey, CA 93940
   Reference CRO #_____.

International Customers:

Equipment repair is handled by your local Pro-Log distributor. If you need to contact Pro-Log, the factory can be reached at any time by TWX at 910-360-7082.

LIMITED WARRANTY:

Seller warrants that the articles furnished hereunder are free from defects in material and workmanship and perform to applicable, published Pro-Log specifications for two years from date of shipment. This warranty is in lieu of any other warranty expressed or implied. In no event will Seller be liable for special or consequential damages as a result of any alleged breach of this warranty provision. This liability of Seller hereunder shall be limited to replacing or repairing, at its option, any defective units which are returned F.O.B. Seller's plant. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, unauthorized repair, or installation are not covered by warranty. Seller shall have the right of final determination as to the existence and cause of defect. As to items repaired or replaced, the warranty shall continue in effect for the remainder of the warranty period, or for ninety (90) days following date of shipment by Seller of the repaired or replaced part whichever period is longer. No liability is assumed for expendable items such as lamps and fuses. No warranty is made with respect to custom equipment or products produced to buyer's specifications except as specifically stated in writing by Seller and contained in the contract.

Cut Here

FOLD

FOLD

PRO-LOG® CORPORATION

Yes, I'm interested in Pro-Log.

Please send me more information about your:

- ☐ 7000 Series STD BUS Cards
- ☐ STD BUS Packaging Solutions
- ☐ STD BUS Subsystem
- ☐ STD BUS Systems
- ☐ Designer Software
- ☐ Design Courses and Seminars
- ☐ Programmer Product Line
- ☐ Other _____

- ☐ I am currently using Pro-Log equipment.
- ☐ Add my name to your mailing list.
- ☐ Please have a Sales Representative contact me.

Reader Comments: _____

Name _____ City _____

Company _____ State _____ Zip _____

Address _____ Telephone _____

PLACE
POSTAGE
HERE

PRO-LOG®
CORPORATION
2411 GARDEN ROAD
MONTEREY, CA 93940

Attn: Literature Department